Performance of 100-kV advanced nanoelectron-beam Exposure system, JBX-9300FS, and its application of sub-100-nm CMOS devices

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Device miniaturization

DRAM Generation (GBit)

0.256 1 4 16 64 256

Feature Size (nm)

200

100

70

50

30

10


Product Year

Wafer Size (mm)

500

400

300

200

100

Feature size and wafer size trends according to SIA road map and various institute

NEC
Throughput for various types of Electron beam exposure

- SCALPEL: Scattering angular limitation projection electron beam lithography
- PREVAIL: Projection electron beam lithography with variable axis immersion lens
- EBDW: Cell projection with VSB
- BAA: Blanking aperture array
- VSB: Variable shaped beam

Throughput (8" wafers/hour):
- 10
- 1
- 0.1

Resolution:
- 300nm
- 100nm
- 50nm
- 10nm
Lithography Techniques

Throughput [wafers/hour]

- Mass production
- R&D
- EBDW (Point Beam)
- EBDW (Variable Shaped Beam /Cell Projection)
- EUV*
- F2*
- EPL*
- KrF
- Now

*under development

Resolution [nm]

30 50 80 100 130 150

Background

NEC
EB systems used in NEC, Japan

Ohtsu:
JBX-5D II (modified)
JBX-6000FS

Tsukuba:
JBX-5FE
with 12MHz DAC

Sagamihara:
JBX-9300FS
JBX-9000MV
JBX-7000MV
HL-800D
HL-900DX
MEBES

Kyoto
Tokyo
Aim and requirements of our EB system in Sagamihara, NEC

Research and development sub-100nm advanced CMOS

1. Wafer size
   - 12-inch (maximum) wafer available stage.
   - X-ray mask available

2. High-throughput
   - High-frequency deflection
   - Large field
   - In-line developer

3. High-precision lithography
   - High-acceleration energy (100kV)
   - Dynamic focus and dynamic stigma correction with wafer-height measurement
   - Wafer mark detection with self-correlation method
JBX-9300FS installed in NEC Sagamihara

Thermal magnetic shield chamber

100kV column

high-voltage tank

Wafer auto-loader and interface for automatic developer

JBX-9300FS with automatic developer is installed in a thermal shield.

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Progress in introduction of JBX-9300FS at NEC

Dec 1997 start to construction of floor reinforcement and thermal magnetic shield chamber
May 1998 carry in and installation of JBX-9300FS
Aug 1998 first beam at 50 kV

May 1999 finish of installation at 50 kV

June 2000 finish of installation at 100 kV
Automatic developer for 8-inch wafer

- >50 wafers/hour
- developer: TMAH/organic
- chemical filter installed

Mark 8 made by TEL (Tokyo Electron Ltd.)
Specifications of EB system 1

beam type : spot beam
electron source : ZrO / W TFE
Acceleration voltage : 50 / 100kV
Scanning : vector scan
stage movement : step & repeat
wafer size : 6, 8, 12inch, X-ray mask
resolution of laser interferometer : 0.62nm
main deflector DAC : 20 bit
dynamic focus and stigma correction with wafer height measurement : height measurement accuracy 0.1 μm
Specifications of EB system 2

Deflection: 1- and 2-stage available
1-stage for high precision
2-stage for high frequency deflection

Deflection speed: >25MHz

Field size: 1000μm × 1000μm at 50 kV
500μm × 500μm at 100 kV

Sub field: 10μm × 10μm at 50 kV
5μm × 5μm at 100 kV

Beam deflection step: 2nm at 50 kV
1nm at 100 kV

Thermal magnetic shield chamber: controlled at ±0.1°C

in-line automatic developer: for 8 inch wafer

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Inline developer for 8-inch wafer with EB exposure

Chemical amplified resist is available. Continuous operation is performed.

EB column

Exchange chamber

Stage chamber

Wafer auto loader

Automatic developer

8-inch wafer

IN

OUT
X-ray mask cassette

For NIST specified X-ray mask

NEC
4-stage accelerator
Beam stability at 50 and 100kV

(a) 50kV

Current (nA)

<0.1%

(b) 100kV

Current (nA)

<0.1%

10000hrs

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Electron beam diameter dependence on beam current

Calculation results
Beam diameter measurement

(a) knife edge method (50kV, 1nA) (b) beam diameter (calculation)
Beam diameter measurement at 100 kV

dx = 3.6 nm

dy = 4.0 nm
Exposure performance

resist: ZEP520 (positive resist),
thickness: 30nm, developer: amyl acetate
$V_{acc}=50\text{kV}$, $I_b=100\text{pA}$, $420\text{mC/cm}^2$,
2stage deflector

(a) cross pattern

(b) L/S pattern
30-nm width negative resist pattern with 265-nm height

EB: 50kV 200pA (JBX-9300FS)
Resist: NEV22A3 chemically amplified resist
(Sumitomo Chemical Co.)
Standard sensitivity: 9.5 \( \mu \text{C/cm}^2 \)
Wafer: polysilicon/8-inch silicon
PB 110°C for 60sec
with proximity effect correction
\( \alpha=15\text{nm}, \beta=10\text{mm}, \gamma=2.9 \)
with Dynamic focus/Dynamic stigma
scanning field: 1 mm with Height Correction.
PEB 100°C for 60sec
Development: TMAH 2.38% for 60s

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100-nm diameter positive resist pattern with 600-nm height

EB: 50kV 200pA (JBX-9300FS)
Resist: UV5 chemically amplified resist (Shipley Co.)
Exposure dose: 28 μC/cm²
Wafer: 8-inch silicon
PB 110°C for 60sec
with Dynamic focus/Dynamic stigma scanning field: 1 mm with Height Correction.
PEB 145°C for 75sec
Development: TMAH 2.38% for 45s

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Contact hole exposure at a dose of 28 \(\mu\text{C/cm}\) on UV-5 resist

- Resist: UV-5 0.6 \(\mu\text{m}\) thickness
- FB: 50 kV, 196 pA, beam step 2x6=12 nm
- Dose: 28 \(\mu\text{C/cm}^2\)
- Proximity correction: none

Development: PEB 145 C, 75 sec
Developer TMAH(2.38%), 45 sec
0.09 μm L&S pattern for wiring (positive resist) at 50 kV
Wafer mark detection

Requirement for wafer mark detection

- high mark detection accuracy for high-overlay accuracy
- apply for CMOS LSI gate, contact, and wiring lithography

Problem

- mark damage due to device process
- Degradation of S/N on mark signal
- Modification of mark signal

Accumulation of mark detection signal and self-correlation method
Mark detection using accumulation and self correlation method

Detector for backscattered electrons

\[ Z(i) = \sum_{j=j_1}^{j_2} Y(i - j) \cdot Y(i + j) \]

Host computer

Memory

Self-correlation mark center detection

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Mark detection of Au-metal-cross mark

accummulation (50 times)

deferential

self-correlation

Mark detection signal \( V_{acc} = 50kV, I_b = 100pA \)

Mark detection repeatability: \( 2\sigma_x = 5.2\text{nm}, 2\sigma_y = 5.4\text{nm} \)

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Mark detection accuracy by using device pattern

aluminum (w:10mm, t=0.3mm)

50kV EB

0.6mm

SiO₂

Si sub.

(a) cross section of mark sample

(b) mark detection signal (V_{acc}=50kV, I_b=2nA)

Mark detection repeatability: \(2\sigma_x = 25.0\, \text{nm}, \ 2\sigma_y = 24.0\, \text{nm}\)

50 times accumulation
Differential
Self-correlation

NEC
Beam control
Beam position and focus correction system

Subfield scanner correction

Main field correction

Sample height measurement

2-axis laser

1-axis laser

Subfield scanner correction

Main field correction
Overlay exposure

4-alignment mark + Stepper distortion table

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Exposure with distortion correction
Field shift and shot shift exposure

Field shift exposure

1st exposure
Field boundary
2nd exposure

Shot shift exposure
1st exposure
Shot boundary
2nd exposure