Graphic user interface for EB control
Pattern data flow

Design of pattern

→ GDS II (stream) format

→ CAPROX(Sigma-C):
  Pattern modification
  Proximity correction
  Formatting

→ JEOL52V3 format

→ JBX-9300FS

NEC
Field distortion correction of EB overlay exposure on the pattern exposed by optical stepper

**w/o correction**

**with correction**

Overlay error due to stepper distortion

- Designed gate position
- Designed isolation position
- Designed gate position

**correction**
Example of field distortion by i-line stepper

Error for ideal position
★ X_{max} = 32\text{nm}
● X_{min} = -27\text{nm}
Y_{max} = 28\text{nm}
Y_{min} = -27\text{nm}
Distortion correction to obtain high overlay accuracy

- Previous method:
  - correction of field position
  - $X' = X + A0$
  - $Y' = Y + B0$

- Present method:
  - Correction of four field corner
  - $X' = A0 + A1X + A2Y + A3XY$
  - $Y' = B0 + B1X + B2Y + B3XY$

NEC
Performance of stepper distortion correction at 50kV

**w/o correction**

- **X**: Av.= 9nm, 3σ= 35nm
- **Y**: Av.= 24nm, 3σ= 28nm

**with correction**

- **X**: Av.= 11nm, 3σ= 20nm
- **Y**: Av.= 18nm, 3σ= 15nm

**Frequency** vs **Overlay Error [nm]**

*NEC*
EB/DUV Intra-level Mix and Match (IL M&M) Lithography

In EB/DUV IL M&M lithography, EB exposed area decreases, then throughput in EB exposure increases.

NEC
Requirements for sub-100nm CMOS devices by EB/DUV IL M&M lithography

(1) High resolution EB system
(2) High sensitivity and high resolution resist for both EB and DUV
(3) Inter-level and Intra-level overlay accuracy between EB and DUV
(4) correction for mutual interference between EB and DUV
(5) CD uniformity

In this work,
- advanced point electron beam system ⇔(1)
- pattern data preparation ∈ (3)
- resist process ⇔(5)

are focused on.
Exposure characteristics of resists exposed by EB and KrF

- Examined by exposure of isolation line

<table>
<thead>
<tr>
<th></th>
<th>EB</th>
<th>KrF</th>
<th>ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAL606</td>
<td>100nm*</td>
<td>250nm*</td>
<td>M&amp;M by Toshiba</td>
</tr>
<tr>
<td>UVN2,N30</td>
<td>50nm#</td>
<td>180nm$</td>
<td>negative resist for KrF</td>
</tr>
<tr>
<td>NEB22</td>
<td>30nm</td>
<td>?</td>
<td>few roughness</td>
</tr>
</tbody>
</table>

*reported by Toshiba  #reported in paper  $from leaflet
Influence of EB on KrF exposure pattern

- Significant influence by EB backscattered electron ($\sim 10 \ \mu m$)
- Area exposed by EB100% $\rightarrow$ increase on a pattern width of 100 nm exposed by KrF
Resolution test of NEB22A3 exposed by KrF

Designed width: 160nm, 300nm (two-time PEB, w/o BARC), 500nm
KrF exposure characteristics – post bake durability

one-time PEB
two-time PEB

Improvement of pattern width change rate from -2.6nm/hour to -0.5nm/hour by two-time PEB.
Influence of KrF on the pattern exposed by EB

- Influence of KrF is about 50nm
- Increase in line width of about 10% exposed by EB at a distance of 0.1μm
Exposure characteristics of calixarene resist at 50 and 100 keV

The comparison of sensitivity curves of calix[6]arene resist at 50 and 100kV acceleration voltages.
Calixarene resist pattern exposed at 100 kV

SEM photograph of 12nm width resist pattern. Designed width is 5nm and exposed dosage is 100 mC/cm².
CD control performance

The relationships between designed and resist pattern width for various dosages. The inset is an exposed pattern.
Etching durability of calixarene

Etching gas: HBr
poly-Si etching using HBr gas plasma etching with calixarene resist mask.

Designed pattern size is 20nm for lines and 70nm for spaces. Original resist thickness was 100nm.
An example of beam diameter measurement and minimization by using “knife edge” method in JBX-9300FS. Dashed curves show results fitted by approximation calculation.
Performance of dynamic focus and stigma correction in a 500mm large field
Necessity of overlap pattern to avoid disconnection (1)

(a) original pattern

(b) for $\Delta E_y$

$\Delta E = 0$, $|\Delta E_y| > 0$

$\Delta E = 0$, $|\Delta E_y| > 0$

(C) for $\Delta E_x$, $|\Delta E_x| < L$

$\Delta E = 0$, $|\Delta E_x| > 0$

Another overlap pattern is necessary when $|\Delta E| < L$.

$X \uparrow$
$Y \downarrow$

$\Delta E$: overlay error between EB and DUV
$L$: gate length

Data preparation

NEC
Method for making longitudinal overlap

Original pattern
\[ \Delta W (> DE) \]
Parallel movement

[AND]

\[ \Delta W (> \Delta E) \]
EB data with overlaps

This method provides overlaps with arbitrary size independent of feature size.

Data preparation
Necessity of overlap pattern to avoid disconnection (2)

(d) for $\Delta E_x$, $|\Delta E_x| > L$ (when $L$ is smaller than overlay error)

For CMOS devices, low $I_{on}$?

$\Delta E = 0$, $|\Delta E_x| > 0$

Longitudinal overlap

Longitudinal and lateral overlap

$\Delta E = 0$, $|\Delta E_x| > 0$, $|\Delta E_y| > 0$

Necessary of longitudinal and lateral overlap when $|\Delta E| > L$.

$\Delta E = 0$, $|\Delta E_x| > 0$, $|\Delta E_y| > 0$

w/o device performance degradation

Data preparation
Method for making parallel overlap

ΔW: parallel movement

+ΔL: Increment (ΔL+L>ΔE)

ΔW: parallel movement

ΔL

ΔW

EB data with overlaps

Data preparation
Necessity of overlaps to avoid pattern disconnection 1

(a) original pattern
← DUV pattern
← EB pattern

(b) definition of overlaps and directions

Y (parallel direction to the gates)

X (perpendicular direction to the gates)

(c) for ΔEy

ΔE=0  |ΔEy|>0  ΔE=0  |ΔEy|>0
For ΔEy, parallel overlaps are effective.

ΔE: relative positioning error

Data preparation
Necessity of overlaps to avoid pattern disconnection 2

(d) for $\Delta E_x, |\Delta E_x| < L$
(e) for $\Delta E_x, |\Delta E_x| > L$

$\Delta E = 0$
$|\Delta E_x| > 0$
$\Delta E = 0$
$|\Delta E_x| > 0$

$\Delta E$: relative positioning error
$L$: gate length
Perpendicular overlaps are necessary.

For CMOS devices, low $I_{on}$?

$|\Delta E| < L$: parallel overlaps are necessary.
$|\Delta E| > L$: parallel overlaps and perpendicular overlaps are necessary.

$\Delta E = 0$
$|\Delta E_x| > 0$
$|\Delta E_x| > 0$

Data preparation
Method for making parallel overlaps

Data preparation
Method for making perpendicular overlaps

<+Y direction>

* \( \Delta W \) \( \Delta L \) \( \Delta W \) \( \Delta L \)

<-Y direction>

** \( \Delta W \) \( \Delta L \) \( \Delta W \) \( \Delta L \)

EB data with overlaps

** mean the subsequent procedure after ** of the former viewgraph.

Data preparation
Resist process of EB/DUV IL M&M Lithography

Which is better, \( EB \rightarrow DUV \) or \( DUV \rightarrow EB \)?

\[ \text{chemically amplified resist} \]
\[ \text{coating} \]
\[ \text{EB} \]
\[ \text{DUV} \]
\[ \text{development} \]

\[ \text{Our choice} \]

**EB exposure is performed after DUV exposure, because the influence on the line width variation caused by PED appears especially for EB patterns, which are more critical than DUV patterns.**
Post exposure delay effect for KrF patterns

-2.7nm/hour  \rightarrow  -0.5nm/hour

By adding another PEB before EB exposure

Process
Mix & Match process: two-times PEB for KrF exposure

- NEB22
  - KrF
  - Delay in Air
  - PEB
  - Develop
  - -2.7nm/hour

- NEB22
  - KrF
  - Delay in Air
  - PEB
  - Develop
  - -0.5nm/hour

- NEB22
  - KrF
  - PEB
  - EB
  - Develop

Resist Process

NEC
Process conditions in our EB/DUV IL M&M lithography

1. Resist coating
   NEB22A3 350nm
2. Pre Bake
   110°C× 60s
3. KrF exposure
   Dose=20mJ /cm², F.O.=0.0mm
4. Post Exposure Bake 1
   100°C× 60s
5. EB exposure
   Vac=50kV, I=200pA,
   Beam diameter=7nm
   standard dose=10.8mC/cm²
6. Post Exposure Bake 2
   100°C× 60s
7. Development
   TMAH(2.38%)× 60s
8. Post Bake
   100°C× 60s

In EB exposure, proximity effect correction is performed on the assumption that KrF exposure have no influence on EB-exposed region.
The effect of EB/DUV IL M&M lithography

Result of EB/DUV IL M&M
The effect of EB/DUV IL M&M lithography

Result of EB/DUV IL M&M

NEC
CD control performance on negative resist at 50 kV

![Graph showing the relationship between designed gate length (nm) and resist gate length (nm). The graph is a straight line with points plotted along it, indicating a linear relationship.]
Resist is thinned by about 10nm after EB/DUV IL M&M lithography, and then gate poly-Si is etched. Sub-50nm CMOS devices with high drain current were obtained.
Summary

- We have introduced 100/50kV advanced point EB system with automatic developer.
- We have confirmed high resolution capability with good overlay accuracy.
- We have developed EB/DUV IL M&M lithography to expose the gate layer of sub-100nm CMOS devices.
- Sub-50nm CMOS devices with high drive current were obtained.
- This technology will be applied to the research on the advanced CMOS devices and circuits.
References