Fabrication of 30 nm gate length electrically variable shallow-junction metal–oxide–semiconductor field-effect transistors using a calixarene resist

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(Received 27 May 1997; accepted 27 August 1997)

We have fabricated electrically variable shallow-junction metal–oxide–semiconductor field-effect transistors (EJ-MOSFETs) with an ultrafine gate for the first time. The gate length was reduced to 32 nm by using electron-beam lithography with a calixarene resist, which has an under 10 nm resolution with a sharp pattern edge. Moreover, normal transistor operation of 32 nm gate-length EJ-MOSFETs was confirmed. © *1997 American Vacuum Society*. [S0734-211X(97)16706-3]

I. INTRODUCTION

Recent progress in Si fabrication technologies enables device miniaturization that results in high switching speed and highly integrated circuits of metal–oxide–semiconductor field-effect transistors (MOSFETs). Up to now, the minimum gate length of Si-MOSFETs was 40 nm, which was achieved by electron beam (EB) lithography with a chemically amplified resist[1] or by an exicimer stepper and a resist thinning process.[2] Forty nm gate length MOSFETs operate normally at room temperature and are governed by macroscopic device theory based on a drift–diffusion model. When the gate length is further decreased to less than the 40 nm regime, several physical phenomena, for example, direct source to drain tunneling, interband tunneling at the drain edge, and spatial threshold voltage fluctuations associated with the limited number of impurities, can become detrimental to normal transistor operation. Therefore, it is important to investigate the physical phenomena in this regime and test the feasibility of normal MOSFET operation.

In developing ultrashort-gate length devices, there are mainly two difficulties. The first is suppressing short-channel effects and the second is fabricating an ultrashort gate. To suppress short-channel effects, shallow source and drain junctions are necessary. For the 40 nm gate length device, shallow junctions with a depth of 10 nm were formed by solid-phase diffusion from phosphorus-doped silicated glass.[2] The short-channel effects can also be suppressed in a sub-0.1-μm gate length regime by using an inversion layer that is electrically induced by gate bias.[3] In previous work, we discussed by numerical simulation that this technique is effective even in the 10 nm regime since the junction depth of the inversion layer can be reduced to less than 5 nm.[4] We also proposed an electrically variable shallow-junction MOSFET (EJ-MOSFET) with electrically induced ultrashallow source/drain regions, and calculated the transistor characteristics in the 10 nm gate length regime. The second difficulty is ultrashort-gate fabrication. Recent progress in EB lithography has made 10 nm patterning possible by using calixarene resist. Calixarene is a negative EB resist which has exhibited a resolution of under 10 nm with a sharp pattern edge.[5]

In this article, we have applied EB lithography and a calixarene negative resist to fabricate an ultrafine poly-Si gate. A 32 nm gate length has been achieved for the first time. Further, we confirm the normal operation of a 32 nm gate length device at room temperature.

II. DEVICE STRUCTURE AND FABRICATION PROCESS

Figure 1 shows a schematic cross section of an EJ-MOSFET, which has a lower gate and an upper gate separated by an integrate oxide. When a positive voltage is applied to the upper gate, the shallow source and drain regions are electrically induced at the p-type Si surface. When the lower gate is grounded, the drain current is suppressed by a potential barrier beneath the lower gate. When a positive voltage is applied to the lower gate, the two channel regions are connected electrically. By using the lower gate MOSFET characteristics are obtained. Since electrically induced source and drain regions are extremely shallow, short-channel effects can be suppressed. This structure is not suitable for real device applications because of the parasitic capacitance between the upper gate and the lower gate. Nonetheless, it is useful for investigating physical phenomena in a small-scale regime.

EJ-MOSFETs were fabricated following the process sequence shown in Fig. 2. The starting material was p-type Si with a carrier concentration of 2×10^{18} cm^{-3} on the surface, which was doped by boron ion implantation and drive in. The doping concentration is very important to the transistor characteristics. To suppress short-channel effects, the concentration should be large. However, when the doping concentration is larger than 10^{18}/cm^{-3}, the barrier width increases abruptly. We optimized the value by numerical simulation.[4] The source and drain contact regions were doped by arsenic ion implantation.

A 50-nm-thick field oxide was formed and a 5-nm-thick gate oxide was grown by thermal oxidation at 850 °C. Following this process, an ultrafine poly-Si lower gate was fabricated using a calixarene resist. Details of the procedure for fabrication of the lower gate will be discussed later. The poly-Si lower gate and the Au/Al upper gate were separated by a 24-nm-thick chemically vapor deposited (CVD) SiO_2 layer. To improve the breakdown field of CVD-SiO_2, anneal-

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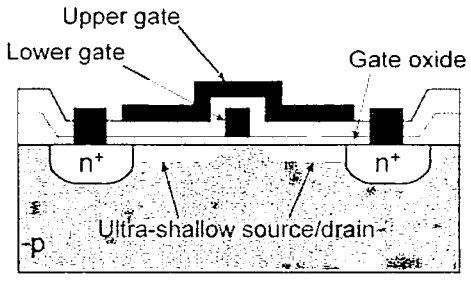

FIG. 1. Schematic cross section of an EJ-MOSFET.

ing was carried out in N_2 at 900 °C and in H_2 at 450 °C. With this procedure the breakdown field increased to 10 MV/cm, which is comparable to that of a thermally oxidized film. Then Au/Al was evaporated.

III. LOWER GATE FABRICATION

Device performance is characterized mainly by the lower gate length. To get an ultrafine lower gate, a patterning technique with an under 10 nm resolution and a gate material with a smooth surface and low resistivity are needed. Our lower gate was fabricated from doped poly-Si film. Poly-Si with a thickness of 35 nm was grown by CVD and was doped in a $POCl_3$ atmosphere. During the doping procedure poly-Si bumps grow up, resulting in residual poly-Si islands or gate length fluctuation after etching. The height and density of the bumps depend on the diffusion conditions. When the diffusion temperature or diffusion time is reduced, the maximum height of the poly-Si bumps becomes smaller, but the sheet resistance of poly-Si becomes larger. Figure 3 shows the height of the bumps and the sheet resistance of the doped poly-Si film for various diffusion times at 850 °C. With decreasing diffusion time, the height of bumps decreased linearly. On the other hand, when the diffusion time is shorter than 10 min, the sheet resistance become higher abruptly. This means that for the poly-Si 10 min is the optimal time.

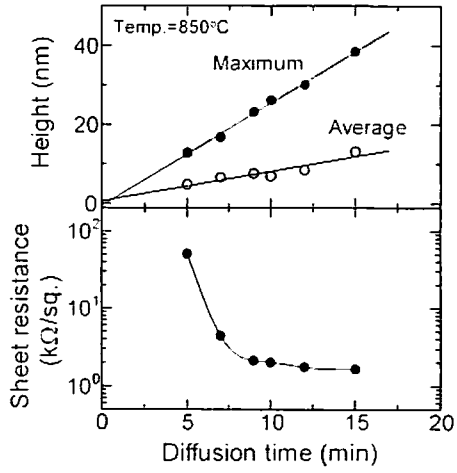

FIG. 3. Diffusion time dependence of maximum height (closed circles) and average height (open circles) of poly-Si bumps on a 5×5 μm^2 Si surface and sheet resistance of the doped poly-Si film.

Following the doping procedure, calixarene resist with a thickness of 50 nm was spin coated on doped poly-Si film and prebaked at 170 °C for 60 min. EB lithography with a beam diameter of 5 nm was carried out for patterning the poly-Si lower gate. The EB dose and acceleration energy were 80 mC/cm^2 and 50 keV, respectively. After the development procedure, the resist pattern was transferred into poly-Si by reactive-ion etching with CF_4 gas. The rf power and the gas pressure were 100 W and 5 Pa, respectively. The resulting etch rate of Si and the etching selectively against SiO_2 were 20 nm/min and 3, respectively. Figure 4 shows the

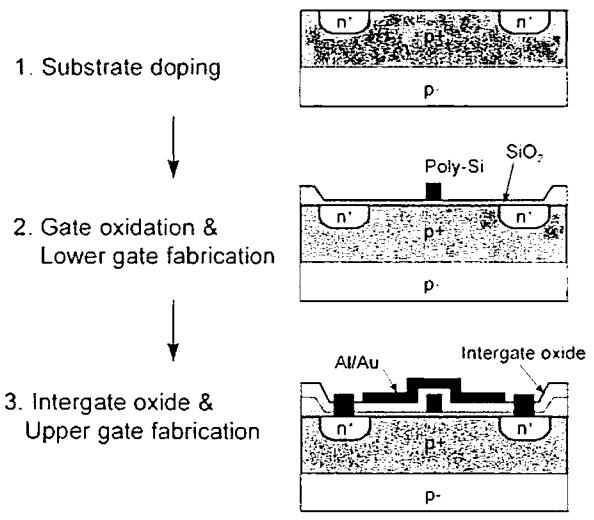

FIG. 2. Fabrication process and schematic cross section of each process for 30 nm gate length EJ-MOSFETs.

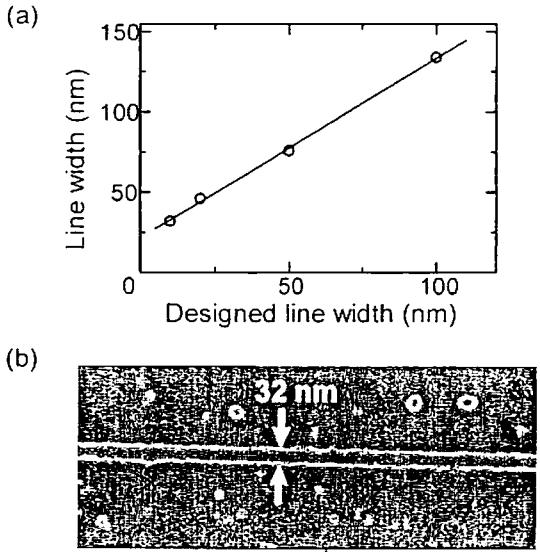

FIG. 4. (a) Linewidth of a poly-Si lower gate vs the linewidth designed. (b) Top view of a lower gate with gate length of 32 nm.

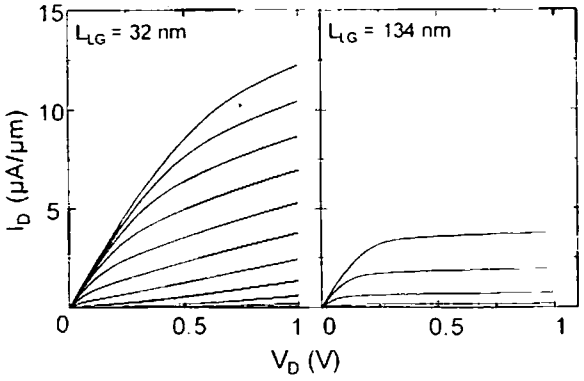

FIG. 5. Drain current vs drain voltage (I_D–V_D) characteristics of EJ-MOSFETs with a lower gate length (L_{LG}) of 32 nm (solid lines) and 134 nm (dotted lines) at room temperature. The upper gate voltage (V_{UG}) was fixed at 18 V and the lower gate voltage (V_{LG}) was biased from 0 to 1.5 V in 0.1 V steps.

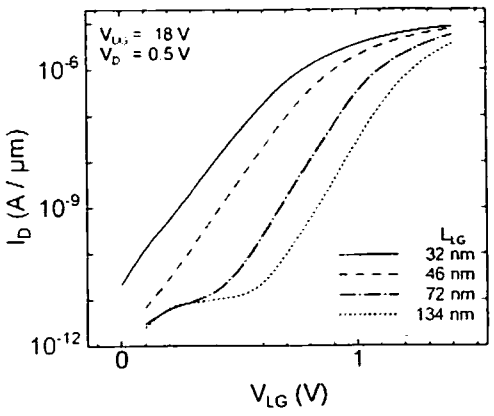

FIG. 6. Subthreshold characteristics for various lower gate lengths (L_{LG}) of 32, 40, 72, and 134 nm. The drain voltage (V_D) and upper gate voltage (V_{UG}) were fixed at 0.5 and 18 V, respectively.

linewidth of the poly-Si lower gate versus the linewidth designed. Since the EB dose was much larger than a threshold dose of the calixarene resist and proximity effects occurred, the width is larger than the designed one. The scanning electron microscopy (SEM) image shows the poly-Si lower gate with a gate length of 32 nm. Although residual poly-Si bumps still exist around the line, an ultrafine lower gate can be fabricated.

IV. DEVICE CHARACTERIZATION OF EJ-MOSFETS

The upper gate voltage (V_{UG}) should be high, since the width of the barrier beneath the lower gate becomes narrow and the source or drain resistance becomes small with increasing V_{UG}. However, V_{UG} is limited by the breakdown field of the intergrate oxide. In the following measurement, V_{UG} was fixed at 18 V. Figure 5 shows the drain current versus the drain voltage (I_D–V_D) characteristics of EJ-MOSFETs with gate lengths (L_{LG}) of 32 and 134 nm at room temperature. The lower gate voltage (V_{LG}) was biased from 0 to 1.5 V in 0.1 V steps. For the device with L_{LG} = 134 nm, there were no short-channel effects. For shorter gate length, although short-channel effects are observed, EJ-MOSFETs operate quite normally. The enhancement of the drain current for a shorter gate length device is mainly due to the decrease in the threshold voltage of the upper gate.

Figure 6 shows the subthreshold characteristics for various values of L_{LG} at room temperature. Below the threshold voltage, I_D was suppressed to less than 20 pA/μm for all the devices and good cutoff characteristics were obtained. When V_{LG} increases, I_D increases exponentially and then becomes saturated at around 10^5 A/μm due to a large parasitic resistance in the source and drain regions. All curves exhibit similar characteristics except for the threshold voltage. This indicates that subthreshold characteristics are mainly governed by macroscopic principles even in the 30 nm gate length regime.

V. CONCLUSION

For ultrafine lower gate EJ-MOSFETs, doping conditions of the poly-Si film are optimized and a 32 nm gate length is achieved by using EB lithography with a calixarene negative resist. We confirm that the EJ-MOSFETs fabricated operate normally in the 30 nm regime and short-channel effects are suppressed very well since the junction depth of the source and drain regions is extremely shallow. Furthermore, no microscopic phenomena detrimental to transistor operation are observed.

ACKNOWLEDGMENTS

The authors wish to thank Jun'etsu Sone for the Si fabrication, and Shinji Matsui and Jun'ichi Sone for their valuable discussions and continuous encouragement. This work was performed under the management of FED as a part of the MITI R&D of Industrial Science and Technology Frontier program (Quantum Functional Devices Project) supported by NEDO.

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