Jpn. J. Appl. Phys. Vol. 39 (2000) pp. 6843–6848
Part 1, No. 12B, December 2000

Intra-Level Mix-and-Match Lithography Process for Fabricating Sub-100-nm Complementary Metal-Oxide-Semiconductor Devices using the JBX-9300FS Point-Electron-Beam System

Mitsuru NARIHIRO*, Hitoshi WAKABAYASHI, Makoto UEKI, Kohichi ARAI, Takashi OGURA, Yukinori OCHIAI and Tohru MOGAMI

System Devices and Fundamental Research, NEC Corporation, 1120 Shimokuzawa, Sagamihara, Kanagawa 229-1198, Japan

(Received July 28, 2000; accepted for publication October 10, 2000)

To increase the throughput of electron beam lithography used to fabricate sub-100-nm patterns, we developed an electron beam and deep UV intra-level mix-and-match lithography process, that uses the JBX-9300FS point-electron-beam system and a conventional KrF stepper. Pattern data preparation was improved for sub-100-nm patterns. To reduce the effect of line width variation caused by post-exposure delay on complementary metal-oxide-semiconductor (CMOS) devices, we first exposed KrF patterns and then added another post-exposure bake before the electron beam (EB) exposure. We have used this technique to expose the gate layer of sub-100-nm CMOS devices. When we set the threshold size between EB and KrF patterns at 0.16 μm, the throughput of electron beam lithography was about threefold that of the full exposure by the electron beam lithography process. Sub-50-nm CMOS devices with high drive current were successfully fabricated.

KEYWORDS: electron beam lithography, KrF, mix and match, overlap, throughput, CMOS

1. Introduction

The rapid shrinking in size of complementary metal-oxide-semiconductor (CMOS) devices has increased the demand for the development of a method to fabricate sub-100-nm patterns. Several lithographic processes, such as F_2 excimer laser lithography with resolution-enhanced techniques (RETs), electron-beam projection lithography (EPL), and X-ray lithography have been proved to have a resolution of less than 100 nm, but they have not been developed sufficiently for practical use. Electron-beam direct writing (EBDW) lithography, using point-electron-beam, variably shaped beam, and cell projection, is an established technique. It has been applied to the limited production of application-specific integrated circuits (ASICs), microwave monolithic integrated circuits (MMICs) and the fabrication of advanced CMOS devices.[1] However, EBDW lithography has a lower throughput than desired, even though it is used in research and development. Nowadays, when we want to fabricate a pattern smaller than 50 nm for use in research on advanced CMOS devices, we cannot help but choose EBDW lithography using a point-electron-beam. This has created a serious problem for researchers because it has the lowest throughput among EBDW lithographic processes.

To improve EBDW throughput, EB/deep UV (DUV) intra-level mix-and-match (IL M&M) lithography was developed and demonstrated.[2–8] It combines EBDW and DUV lithographic processes. The usual (inter-level) mix-and-match lithography also combines EBDW and DUV lithographies, but in this technique they are used to separately expose the different layers. For example, a field layer is exposed using the DUV process and a gate layer is exposed using the EBDW process. In EB/DUV intra-level mix-and-match lithography, EBDW and DUV processes are both used to expose the same layer. For example, one part of the gate layer is exposed using DUV and the other part is exposed using EBDW. In EB/DUV IL M&M lithographic process, the patterns larger than the optical resolution are exposed using DUV and the rest are exposed using EBDW. After both exposures, the resist is developed. The use of EB/DUV IL M&M lithography is very attractive because it can produce patterns smaller than the optical resolution limit and it has a higher throughput than that of the full exposure by EBDW due to the smaller EB-exposed area. Several groups have reported on the resist process in EB/DUV IL M&M lithography and its usefulness for CMOS fabrication. However, the target dimension of many of these groups was 100 nm or larger.

We report that EB/DUV IL M&M lithography can be used for the fabrication of sub-100-nm CMOS devices. To expose the gate layer of sub-100-nm CMOS devices using EB/DUV IL M&M lithography, some requirements must be met. For example, use of a high-resolution EB machine and a high-resolution and high-sensitivity resist, for both the EB and DUV exposures, correction for the mutual interference of the EB and DUV exposures, inter- and intra-level overlay accuracy between the two, and critical dimension (CD) control of the EB and DUV patterns. In this paper, we focus in particular on using an advanced point-electron-beam system, JBX-9300FS,[9,10] as a high-resolution EB machine, a suitable pattern preparation method for sub-100-nm CMOS devices, which we call versatile pattern division and overlap creation method (VEDOC), to prevent pattern disconnection caused by intra-level overlay errors between the EB and DUV patterns, and a resist process to increase CD uniformity. We explain these technologies and describe the results of an experiment using the EB/DUV IL M&M lithographic process developed by us.

2. JBX-9300FS Point-Electron-Beam System

JBX-9300FS was developed by JEOL in cooperation with NEC for the fabrication of advanced CMOS devices. It is used to expose patterns on 8-inch and 12-inch wafers, so that the latest process machines for sub-100-nm CMOS devices can be used. Figure 1 and Table I respectively show a photograph of the JBX-9300FS system and its major specifications. The system features a point beam, a vector scan, and a step-and-repeat stage system. A fine-beam diameter and large field size are achieved at the same time by using dynamic focus and stigma. The maximum scanning clock frequency has been raised by a factor of two compared with the

*E-mail address: m-narihiro@bu.jp.nec.com

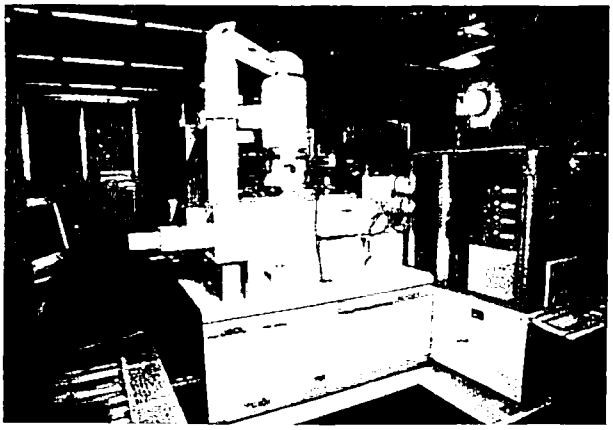

Fig. 1. Photograph of the JBX-9300FS point-electron-beam system, set in a thermal-magnetic-shield room.

Table I. Major specifications of JBX-9300FS.

Acceleration voltage	100 kV	50 kV
Field size (max.)	500 μm	1000 μm
Sub deflection size (max.)	4 μm	8 μm
Beam diameter (I = 100 pA)	4 nm	7 nm
Beam step (min.)	1 nm	2 nm
Laser-interferometer resolution	0.62 nm	←
Main deflector DAC	20 bit	←
Sub deflector DAC	12 bit	←
Deflection speed	25 MHz	←

JBX-6000FS point-electron-beam machine. As a result, JBX-9300FS is one of the best systems in terms of throughput of point-electron-beam machines.

The JBX-9300FS system is connected to an in-line developer through an auto-loader and wafer set apparatus. This setup enables us to develop a chemically amplified resist (CAR) immediately after EB exposure without the affect of post-exposure delay (PED). We can operate this system continuously to expose wafers in volume.

For use in EB/DUV IL M&M lithography, our system has the advantage of being able to fabricate fine patterns smaller than 50 nm in size,[10] and it is unaffected by PED after EB exposure. Continuous operation also contributes to the total throughput.

3. Pattern Data Preparation

In EB/DUV IL M&M lithography, pattern disconnection is a critical problem to be overcome for CMOS devices to operate. Since EB and DUV patterns are displaced more or less from their designed positions due to their respective overlay errors, both patterns can become disconnected at their borders. Therefore it is necessary to add overlaps to the EB patterns and/or DUV patterns to ensure that both are connected.

In our process, overlaps are added to the EB patterns, then all overlaps are positioned on the DUV patterns, so we do not have to change the original design. However, the EB exposed area increases slightly and the throughput of the EB exposure decreases slightly, compared with the exposure of EB patterns without any overlaps.

The relative position error between EB and DUV patterns, ΔE, is an important parameter. The necessary areas of the overlaps and their position depend on the relationship between gate length L and ΔE, as shown in Fig. 2. In the following explanation, we use the example pattern shown in Fig. 2(a) and define the X-direction as the direction perpendicular to the gate and the Y-direction as the direction parallel to the gate. For ΔE_y (the y component of ΔE), parallel overlaps are necessary to avoid pattern disconnection, as shown in Fig. 2(c). For ΔE_x (x component of ΔE), when $|\Delta E_x|$ is equal or less than L, EB patterns with parallel overlaps are adequate to ensure pattern connection (Fig. 2(d)). However, when $|\Delta E_x|$ is larger than L, perpendicular overlaps are needed to prevent pattern disconnection (Fig. 2(e)). It is preferable to use perpendicular overlaps along with the parallel overlaps, because EB patterns with only perpendicular overlaps need large margins and may cause a decrease in the drive current of CMOS devices when $|\Delta E_y|$ (> 0) occurs, as shown in Fig. 2(f). Thus, to avoid pattern disconnection, in the case of $|\Delta E| \leq L$, only parallel overlaps are necessary; in the case of $|\Delta E| > L$, parallel overlaps and perpendicular overlaps are needed. In the previous work,[7] only the case of $|\Delta E| \leq L$ was discussed.

We explain our method for making the parallel overlaps in the case of $|\Delta E| \leq L$. First we separate the original pat-

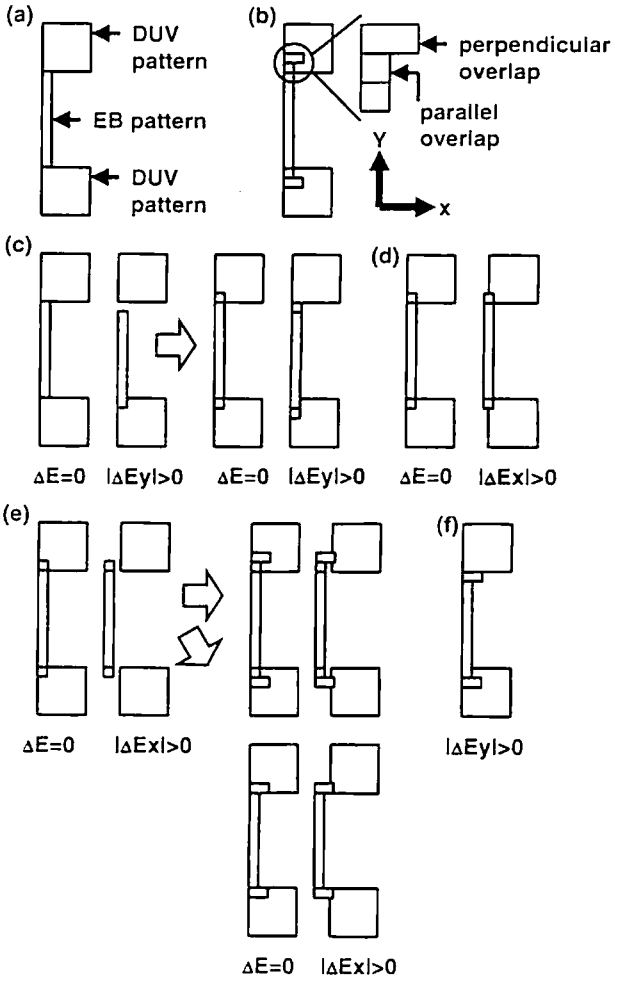

Fig. 2. Necessary overlaps in EB/DUV IL M&M lithography. (a) original pattern, (b) definition of overlaps and directions, (c) necessary overlaps for ΔE_y, (d) necessary overlaps for ΔE_x ($|\Delta E_x| \leq L$), (e) necessary overlaps for ΔE_x ($|\Delta E_x| > L$), and (f) EB pattern with only perpendicular overlaps are displaced.

terns into EB and DUV patterns by using threshold length $L_{th}(>0)$. Usually, we let L_{th} be slightly larger than the resolution limit of DUV lithography, considering factors such as CD distribution, resist cross-sectional shape and resist edge roughness. Original patterns are resized by $-L_{th}/2$ and subsequently by $+L_{th}/2$. The resulting pattern dimensions are larger than L_{th} because the original patterns smaller than L_{th} disappear. These coarse patterns are exposed by DUV. EB patterns are generated by the logical subtraction of the DUV patterns from the original ones.

Next, we make the overlaps parallel to the gates, as shown in Fig. 3. We shift EB patterns by $\Delta W(>0)$ in the $+Y$ and $-Y$-directions. This shifting ensures that EB patterns are extended without changing their size perpendicular to the shift direction. The ΔW is the length of the parallel overlaps and is set to be larger than $|\Delta E|$. The Boolean 'AND' operation between the shifted EB and DUV patterns generates the parallel overlaps, thus, allowing us to make the overlaps only on the DUV patterns. Finally, the parallel overlaps in the $+Y$ and $-Y$-directions are added to the EB patterns and the EB data needed for EB/DUV II: M&M lithography is accomplished. When we use this data, even if a relative positioning error ($|\Delta E_x| \leq |\Delta E| \leq L$, $|\Delta E_y| \leq |\Delta E| < \Delta W$) occurs, we can avoid pattern disconnection without changing the designed size.

Magoshi *et al.*[7] reported another method to obtain EB data with parallel overlaps. However, overlaps cannot be added to the gates with $L \leq \Delta W$ because they disappear after pattern preparation using their method. Therefore, this method cannot be applied to the fine gates. Compared to their method, our method, VEDOC, is complicated because the overlaps are not generated simultaneously. However, our method has the advantage of making arbitrary-sized overlaps without a dependency on minimum EB pattern size. Hence, VEDOC is suitable for fabricating sub-100-nm gate CMOS devices.

In the case of $|\Delta E| > L$, we make the parallel overlaps in the $+Y$ and $-Y$-direction first, followed by the perpendicular overlaps. The method used to make the parallel overlaps is similar to the case mentioned above.

We make the overlaps perpendicular to the gates, using the parallel overlaps, as shown in Fig. 4. The parallel overlaps are displaced by ΔW in the Y-direction and resized by $\pm\Delta L(>0)$. ΔL is the length of the perpendicular overlaps and is determined by satisfying the relationship $L+\Delta L > |\Delta E|$. Then the Boolean 'AND' operation between the extended parallel overlaps and the DUV patterns is performed. The resulting patterns are shifted in the Y-direction and become perpendicular overlaps. Finally, we compile the EB patterns without any overlaps, with parallel overlaps, and with perpendicular overlaps. When we use this data, even if a relative position error ($|\Delta E_x| \leq |\Delta E| < L + \Delta L$, $|\Delta E_y| \leq |\Delta E| < \Delta W$) occurs, we can avoid pattern disconnection without changing the designed gate length.

For the above explanation, we used the pattern shown as an example in Fig. 2(a) for simplicity. The VEDOC method can be used for the patterns in which gates parallel to X-direction as well as Y-direction are involved. The parallel overlaps in $+X$, $-X$, $+Y$ and $-Y$-directions can be made separately as shown in Fig. 5. For the creation of overlaps, the EB patterns are displaced by ΔW, and then the Boolean 'AND' operation between the shifted EB patterns and the DUV patterns is performed. When the perpendicular overlaps in $+X$, $-X$, $+Y$ and $-Y$-directions are necessary to prevent the disconnections as shown in Fig. 2(e), they are also made separately by using the parallel overlaps after the parallel overlaps are

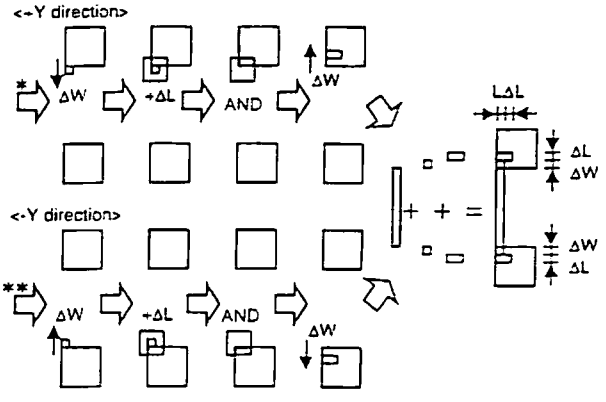

Fig. 4. Pattern preparation method, VEDOC, for $|\Delta E| > L$. Perpendicular overlaps are made from parallel overlaps. * and ** denote the procedure after * and ** of Fig. 3.

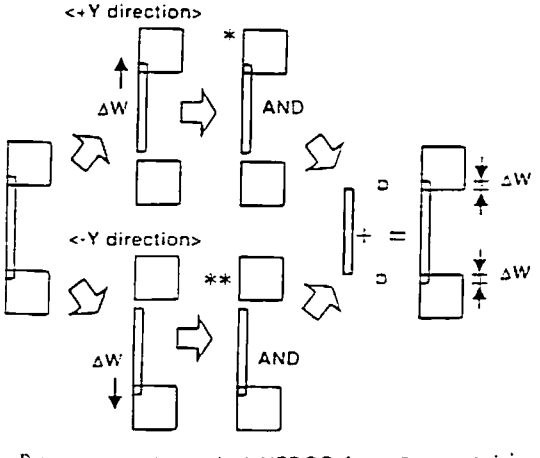

Fig. 3. Pattern preparation method, VEDOC, for $|\Delta E| \leq L$. Parallel overlaps are added to EB patterns.

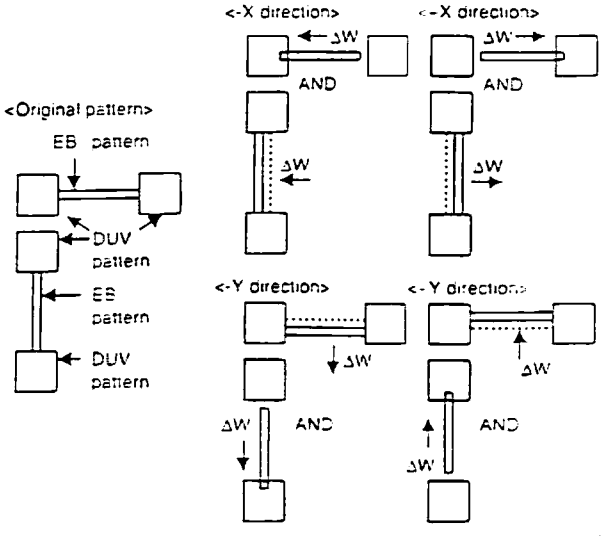

Fig. 5. Pattern preparation method, VEDOC, applied to the patterns which contain the gates parallel to X-direction and to Y-direction.

generated. Then, the final EB patterns are obtained by combining all the created overlaps and the original EB patterns.

4. Experimental Evaluation on Resist Process

We use CAR to increase the throughput of the EB exposure. It is well known that PED has a significant effect on the shape and line width of the developed CAR. When using a CAR in the IL M&M process, we cannot avoid the effect of PED because we have to perform two exposures sequentially.

Since line width variations caused by PED appear, in particular for EB patterns, which are more critical than DUV patterns, we tried to minimize the delay after EB exposure. We decided to expose the DUV patterns first followed by the EB patterns, though the previous works[3,4,6,7] adopted a different exposure sequence. After EB exposure, the resist is developed immediately using an in-line developer. In our exposure sequence, PED after DUV exposure can pose a serious problem.

We investigated the influence of PED after DUV exposure experimentally. We used NEB22A3 negative EB resist (Sumitomo Chemical) as the CAR because it had demonstrated excellent performance in our EB system.[10] Since we wanted to create EB patterns to be as small as possible, no antireflective layer was used. We used a conventional KrF stepper for DUV exposure, an in-line developer connected to the JBX-9300FS for the post-exposure bake (PEB) and development, and a critical dimension scanning electron microscope (CD-SEM) for the line width measurement.

We performed our experiment under the conditions denoted by the insets of Fig. 6. After coating an NEB22A3 resist on an 8-inch Si sample wafer to a thickness of 350 nm and baking it at 110°C for 60 s, we exposed the line-and-space patterns using a KrF stepper. Then we varied the PED time in air after KrF exposure and investigated the dependence of line width on PED. The PED time in air after KrF exposure corresponded to the waiting time before EB exposure and to the EB exposure time. We performed PEB at 100°C for 60 s and developed the sample using Tetramethyl-ammonium hydroxide (TMAH, 2.38%) for 60 s. We found that NEB22A3 resist had good sensitivity for DUV and that line width variations caused by the PED were −2.7 nm/h, as shown in Fig. 6.

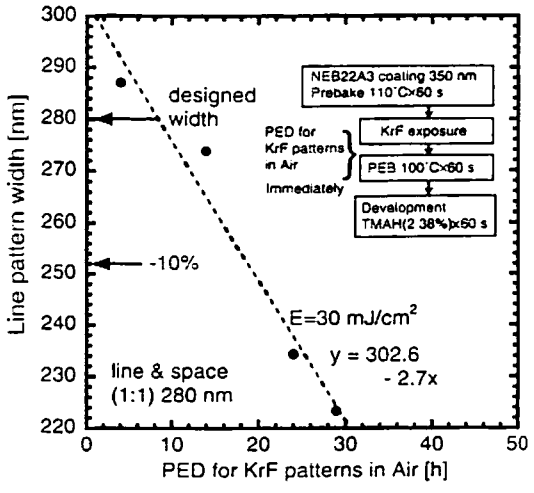

Fig. 6. The effect of PED in air after KrF exposure. The insets show the experimental conditions.

These variations are too large for fabricating sub-100-nm gate CMOS devices because EB exposure takes about 2 h to expose one sample wafer and about one day to expose all the samples.

Next, we investigated the PED effect under the conditions shown in the insets of Fig. 7. These conditions differ in that another PEB sequence at 100°C for 60 s is added after the KrF exposure. This was done to generate the cross-linking reaction in the CAR and to form a latent image before the acid generated by the KrF exposure was neutralized. In this experiment, PED was defined as the interval between the two PEBs. Figure 7 shows that resist sensitivity increased due to the total increase of PEB time, and that line width variations were significantly improved to −0.5 nm/h.

Based on the above results, we determined the sequence for our IL M&M process, as shown in Fig. 8. After the NEB22A3 resist was coated on the Si wafer to a thickness of 350 nm and then baked at 110°C for 60 s, DUV exposure using a KrF stepper was performed. When the DUV exposure was completed, a first PEB procedure was started immediately at 100°C for 60 s. Then EB exposure using the JBX-9300FS was carried

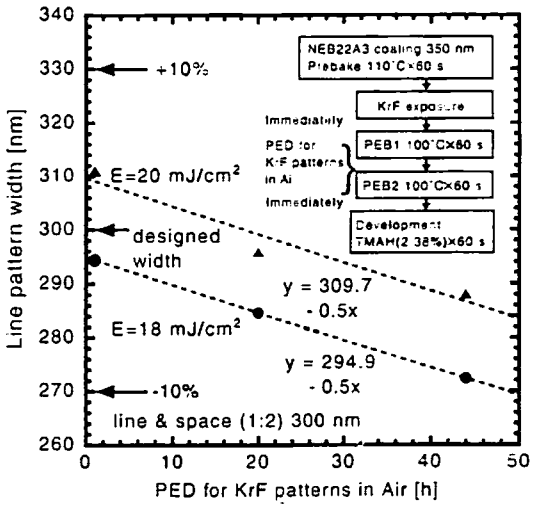

Fig. 7. The effect of PED in air after KrF exposure. The insets show the experimental conditions. A second PEB sequence was added after KrF exposure.

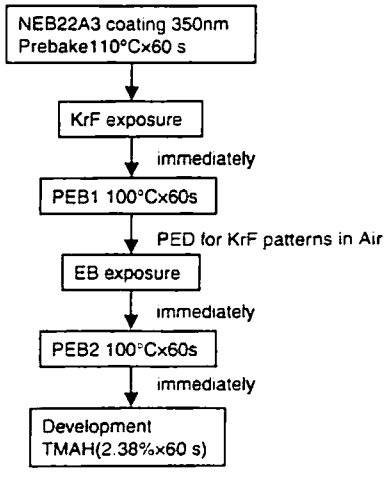

Fig. 8. Final sequence of EB/DUV IL M&M lithography process flow.

out. When the EB exposure was completed, a second PEB procedure at 100°C for 60 s was performed, followed immediately by the TMAH development for 60 s.

5. The Results of EB/DUV IL M&M Lithography

We used EB/DUV IL M&M lithography to expose the gate layer of sub-100-nm CMOS devices. The scanning electron microscope (SEM) photographs in Fig. 9 show two resist patterns formed using our process. For the EB exposure, the acceleration voltage, beam current, beam diameter, and standard dose are 50 kV, 200 pA, 7 nm, and 10.8 μC/cm^2, respectively. Proximity-effect correction (PEC) was performed on the assumption that KrF exposure had no effect on the EB patterns. Strictly speaking, this assumption is not true because the EB- and KrF-exposed regions have an affect on each other.[11] However, in reality it is difficult to calculate these effects precisely because the EB- and KrF-exposed patterns have overlay errors. Therefore, we assumed the above to avoid the worst case, where the gate length near the borders between the EB- and KrF-exposed patterns is too narrow. In actual samples, it was slightly larger than the designed length for the energy given by KrF exposure. For example, in the case of a gate whose designed width was 40 nm, the gate length 100 nm from the gate pad was ~50 nm. However, when the distance from the gate pad to the measured points was longer than 200 nm, the gate length was within ±10% of the designed length. Figure 10 shows that good gate length control was realized down to the sub-50-nm region.

Regarding the throughput of our process, when we set L_{th} at 0.16 μm, the EB exposed area reduced to about 1/6, and the EB exposure time reduced to about 1/3, for EBDW only.

Figure 11 shows the threshold voltage V_{th}-physical gate length L_g characteristics of CMOS devices, whose gate layer

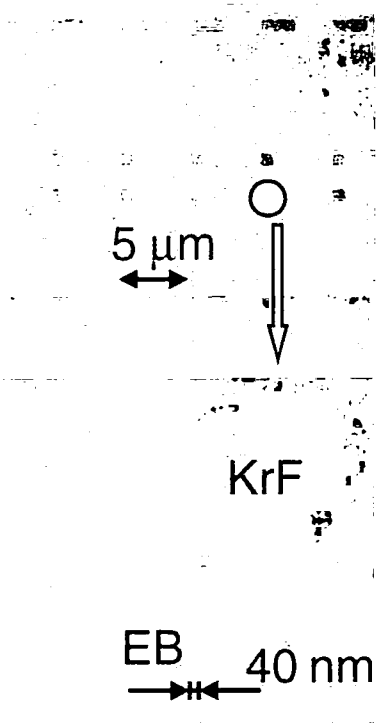

Fig. 9. SEM photographs of resist patterns formed by EB/DUV IL M&M lithography. They were taken before resist thinning. Ring oscillator with a 40 nm gate length was fabricated.

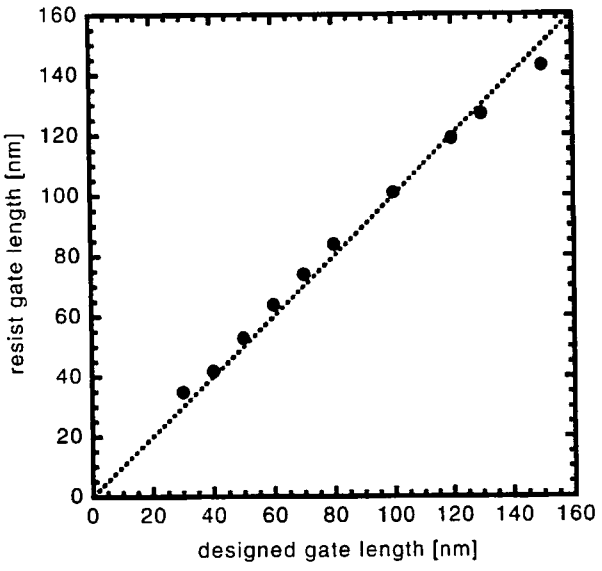

Fig. 10. The relation between the designed gate length and the resist gate length before thinning. Gate length was measured at the point free from the influence of KrF exposure. The dashed line is an eye-guide and shows that the designed gate length is equal to the resist gate length.

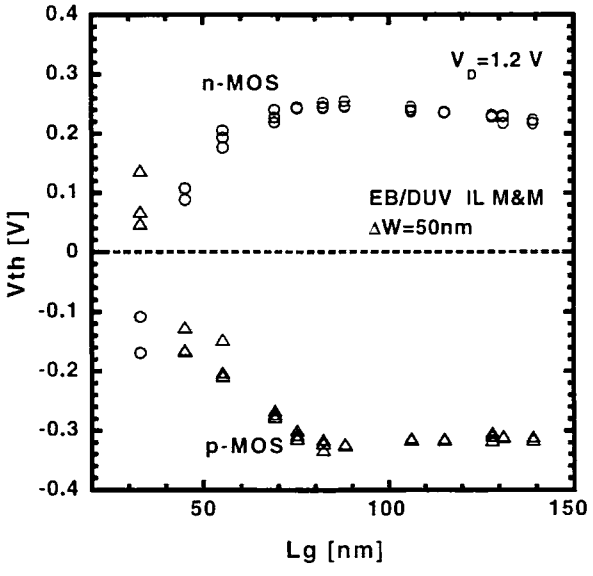

Fig. 11. V_{th}-L_g characteristics of fabricated CMOS devices. The gate layer was exposed using EB/DUV IL M&M lithography. The other layers were exposed using optical lithography. The experimental data obtained from three chips on the same wafer are plotted. The gate patterns of the CMOS devices in this figure did not have the flag-shaped patterns. We added only the parallel overlaps.

was exposed using our process. After the exposure of the gate layer, the developed resist patterns were thinned by about 10 nm in total by plasma etching and the gate poly-Si was etched. Smooth V_{th} lowering was observed, as shown in Fig. 11, showing that the gates were fabricated properly down to the sub-50-nm region without any large distribution. This meant that the parallel overlaps with $\Delta W = 50$ nm worked effectively and that among the devices measured there were no disconnections between the gates exposed by EB and the gate pads exposed by DUV. Figure 12 shows the drive current I_{on}-physical gate length L_g characteristics of the CMOS

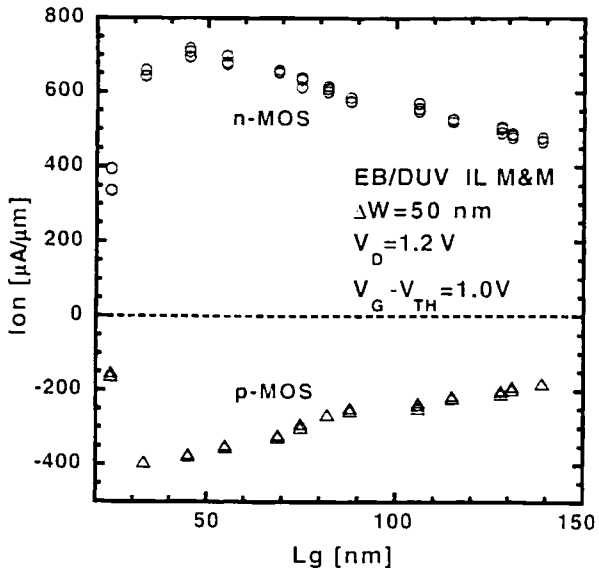

Fig. 12. I_{on}-L_g characteristics of fabricated CMOS devices. The data was obtained from the same devices used for Fig. 11.

devices to be the same as those shown in Fig. 11. High drive current was achieved for these CMOS devices. We found that the CMOS devices with 45-nm gates operated well and had good performance. Detailed process conditions and device characteristics will be reported elsewhere.[12]

6. Conclusion

We used our EB/DUV IL M&M lithography process to expose the gate layer of sub-100-nm CMOS devices, using the JBX-9300FS point-electron-beam system, suitable pattern preparation method, VEDOC, for sub-100-nm patterns, and a process where DUV patterns are exposed first and then a second PEB sequence is added after the DUV exposure. Throughput of the EB exposure in our process was about threefold that for EBDW only. Sub-50-nm CMOS devices with high drive current were fabricated. This technology is applicable for future research on advanced CMOS devices and circuits.

Acknowledgements

We thank Masao Fukuma and Takemitsu Kunio for continuous encouragement, and the members of our laboratory for fruitful discussions. We would like to extend our thanks to Hitoshi Takemura, Hirofumi Ohki and other JEOL members for the improvements made by them to the JBX-9300FS system.

1) H. Wakabayashi, T. Yamamoto, Y. Saito, T. Ogura, M. Narihiro, K. Tsuji, T. Fukai, K. Uejima, Y. Nakahara, K. Takeuchi, Y. Ochiai, T. Mogami and T. Kunio: Very Large-Scale Integration (VLSI) Symp. Tech. Dig. (1999) p. 108.
2) P. Zandbergen and H. Dijkstra: Microelectron. Eng. 23 (1994) 299.
3) R. Jonckheere, A. Tritchkov, V. Van Driessche and L. Van den hove: Microelectron. Eng. 27 (1995) 231.
4) F. Benistant, S. Tedesco, G. Guegan, F. Martin, M. Heitzmann and B. Dal'zotto: J. Vac. Sci. & Technol. B14 (1996) 4051.
5) J. Yamamoto, S. Uchino, H. Ohta, T. Yoshimura and F. Murai: J. Vac. Sci. & Technol. B15 (1997) 2868.
6) S. Tedesco, T. Mourier, B. Dal'zotto, A. McDougall, S. Blanc-Conquant, Y. Quéré, P. J. Paniez and B. Mortini: J. Vac. Sci. & Technol. B16 (1998) 3676.
7) S. Magoshi, H. Niiyama, S. Sato, Y. Kato, Y. Watanabe, T. Shibata, M. Ito, A. Ando, T. Nakasugi, K. Sugihara and K. Okumura: Jpn. J. Appl. Phys. 38 (1999) 2169.
8) A. J. van Dodewaard, W. S. M. M. Ketelaars, R. F. M. Roes, J. A. J. Kwinten, F. C. M. J. M. van Delft, A. J. van Run, A. K. van Laungen-Suurling and J. Romijn: Microelectron. Eng. 53 (2000) 461.
9) Y. Ochiai, T. Ogura and T. Mogami: Microelectron. Eng. 46 (1999) 187.
10) H. Takemura, H. Ohki, H. Nakazawa, Y. Nakagawa, M. Isobe, Y. Ochiai, T. Ogura, M. Narihiro and T. Mogami: Microelectron. Eng. 53 (2000) 329.
11) R. Inanami, T. Nakasugi, S. Sato, S. Mimotogi, S. Tanaka and K. Sugihara: Jpn. J. Appl. Phys. 38 (1999) 7035.
12) H. Wakabayashi, M. Ueki, M. Narihiro, T. Fukai, N. Ikezawa, T. Matsuda, K. Yoshida, K. Takeuchi, Y. Ochiai, T. Mogami and T. Kunio: to be published in Int. Electron Devices Meet. (IEDM) Tech. Dig. 2000.