Cu Single Damascene Interconnects with Plasma-polymerized Organic Polymers (k=2.6) for High-speed, 0.1μm CMOS devices

M. Tagami, T. Fukai, M. Hiroi, J. Kawahara, K. Shiba*, M. Tada, T. Onodera, S. Saito, K. Kinoshita, T. Ogura, M. Narihiro, K. Arai, K. Yamaguchi, M. Fukaishi, K.Kikuta,T. Mogami and Y. Hayashi

System Devices and Fundamental Res., *ULSI Device Development Div., NEC Corporation
1120, Shimokuzawa, Sagamihara, KANAGAWA 229-1198, Japan
TEL: +81-42-771-4267, FAX: +81-42-771-0886

For high-speed CMOS devices, triple-layered Cu single damascene interconnects (SDI) with Cu-via plugs are fabricated in hybrid dielectric films of plasma-polymerized divinylsiloxan benzocyclobuten film (p-BCB: k=2.6) and p-CVD SiO_2. No degradation of 0.1μm MOSFETs is observed after the full interconnect integration through MOCVD-Cu filling and pad-scanning, local-CMP for Cu polish. The stacked Cu-pads in the high modulus p-BCB film (19Gpa) withstand sever mechanical impact during Al wire bonding. The 0.08μm CMOS transmitter, which consists of 32:8 pre-multiplexer (MUX), 8B10B encorder, 10:1 MUX and DATA driver, is obtained successfully to generate high-speed serial signals up to 6Gb/s. This fabrication process is a key to obtain the high speed CMOS devices with low-k/Cu interconnects.

Introduction Since interconnect delay restricts ULSI operation speed, low-k/Cu interconnect technology has been studied extensively [1-2]. Little study, however, has been reported to evaluate the circuit-level performance with multilevel low-k/Cu interconnects because of the poor fabrication yield currently. In this paper, we make a CMOS transmitter [3] with triple-layered low-k/Cu interconnects, which were obtained by the integration of unique process techniques such as plasma-polymerization technique for p-BCB [4], MOCVD-Cu filling technique [5] and pad-scanning, local-CMP (PASCAL-CMP) technique [6]. This process combination has high fabrication feasibility for the high speed CMOS devices.

Process Technology (Fig. 1-4): CMOS transistors with 80nm to 120nm-long (L_{gate}) polysilicon gates were fabricated by direct electron-beam lithography. Here, 1.9nm-thick SiON was used for the gate dielectrics. Then, triple-layered, Cu-SDIs with Cu-via plugs (Cu-VP) were fabricated in hybrid dielectric films of p-BCB (k=2.6) and p-CVD SiO_2(Fig.1). The minimum line-pitch and the via-diameter were designed as 0.56μm-pitch and 0.28μmϕ, respectively. Inline sequential deposition technique of ionized-PVD Ta/TaN and MOCVD-Cu was used taking into considerations of keeping the via-yield high as well as the future extendibility. Here, the thick Ta-film on the amorphous-TaN film was used to get the low via-resistance of 3Ω /unit (Fig. 2), probably due to suppression of highly-concentrated fluorine layer formation in Ta-film during MOCVD-Cu. The Cu-SDI and Cu-VP were obtained by PASCAL-CMP under special condition of low-pressure (0.2kg/cm^2) and high pad-rotation rate (400rpm) (Fig. 3). After the Cu metallization, Al-pads were put on the simply stacked Cu-pads, and Al wire-bondings were made finally. The stacked Cu-pad strucure plugged in the p-BCB film with relatively high modulus (19GPa) is a key to obtain the wire-bonding without delamination (Fig. 4).

CMOS Characteristics (Fig. 5-6): Typical n-MOSFET and p-MOSFET with 0.1μm-long, gates had the on-currents of nMOS|pMOS=690|270μA/μm, and the off-currents of 5nA/μm at Vdd=1.2V. The characteristics of MOSFETs with the triple-layered p-BCB/Cu-SDI, such as V_{th}-L_{gate} and I_{on}-I_{off}, were the same as those with the uncovered single-layered Al interconnects and with the conventional triple-layered p-CVD SiO_2/Cu interconnects (Fig. 5 and 6). This indicates no special process damage on the CMOS transistors by the p-BCB/Cu SDI integration.

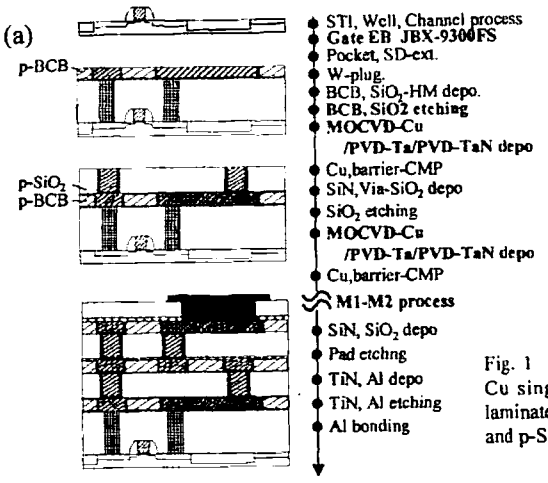
Process Evaluation through High-speed Circuit Fabrication (Fig. 7-10): The effective capacitance for the p-BCB/Cu interconnects were approximately 10% smaller than that for the conventional p-CVD SiO_2/Cu interconnects (Fig. 7). The 101 stages, CMOS ring oscillators (Fun-out (FO) =1) with p-BCB/Cu SDIs was approximately 10% faster than those with p-CVD SiO_2/Cu interconnects (Fig. 8). The 0.08μm CMOS transmitter was fabricated, which consisted of 32:8 pre-multiplexer, 8B10B encorder, 10:1 multiplexer and DATA driver (Fig. 9). A typical waveform is shown in Fig. 10. The transmitter with triple-layered, p-BCB/Cu SDI was confirmed to generate 6Gb/s serial signals by 3GHz-clock signal applied. This indicates the high feasibility of this fabrication process for the high-speed CMOS devices with low-k/Cu interconnects.

Conclusions By combining the plasma-polymerized technique for p-BCB film with MOCVD-Cu filling and PASCAL-CMP for the Cu-polish, the multilevel p-BCB/Cu SDIs with the Cu-via plugs were successfully integrated on the 0.1μm CMOS devices. This process combination enables us to fabricate high speed CMOS devices effectively.

Acknowledgment The authors would like to thank Dr. Michael E. Mills, The Dow Chemical Company, for supplying the DVS-BCB monomer. The authors would like to thank Dr. K. Nakamura, Dr. M. Yamashina, Dr. Y. Ochiai and Dr. T. Kunio, NEC Corporation, for their encouragement and supporting the research.

References [1] R.D. Goldblatt, et al., 2000 International Interconnect Technology Conference (IITC), p261. [2] H. Kudo, et al., 2000 IITC, p270. [3] M. Fukaishi, et al., ISSCC 2000, p260, [4] J. Kawahara, et al., 2000 Symp. VLSI Technology, Technical Digest, p20. [5] M. Tagami, et al., 1999 IEDM, p635. [6] Y. Hayashi, et al., 1999 IITC, p100.

0-7803-6438-4/00/$10.00 ©2000 IEEE



(b)

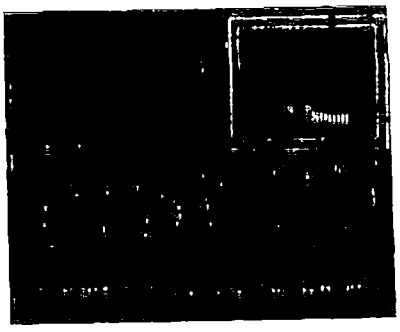


Fig. 1 Fabrication process for 80nm CMOS with triple layered Cu single damascene interconnects with Cu-via plugs in laminated dielectric films of plasma-polymerized BCB (p-BCB) and p-SiO_2; (a) Process flow, and (b) SEM images of 80nm gates.

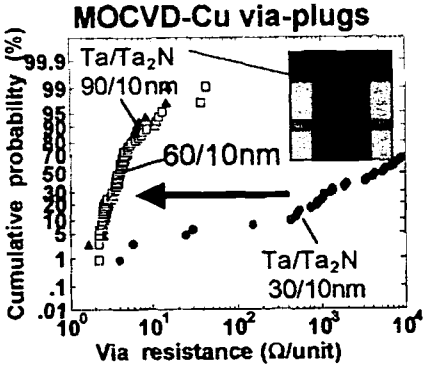


Fig. 2 Effects of Ta-film thickness on MOCVD-Cu via-resistance (0.28μmϕ). The thicker Ta-film accomplishes the low via resistance (3Ω/unit) even though the direct deposition of MOCVD-Cu without PVD flash-Cu.

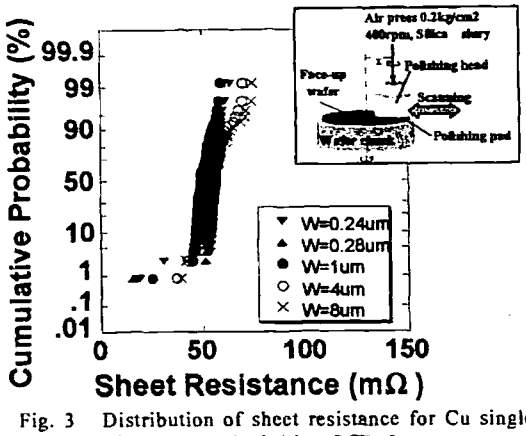


Fig. 3 Distribution of sheet resistance for Cu single damascene interconnects buried in p-BCB. Low pressure and high rotational speed polishing was realized by PASCAL (Pad-scanning, local)-CMP, providing the high uniformity of Cu damascene interconnects in the low-k film..

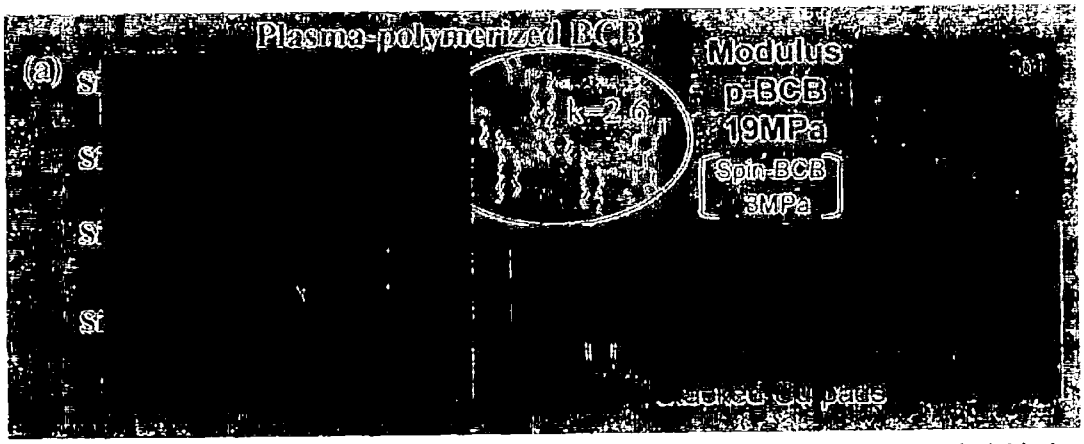


Fig. 4 SEM micrographs of 0.1μm CMOS device with the triple-layered Cu single damascene interconnects buried in the laminated p-BCB(k=2.6)/p-SiO_2 films: (a) a cross-sectional view, (b) a birds-view and (c) a cross-sectional view of Al wire bonding on the stacked-Cu pads. Here, the MOCVD-Cu via-plugs of 3Ω/unit are made in p-CVD SiO_2 film. The stacked Cu-pad strucure plugged in the p-BCB film with relatively high modulus (19GPa) is a key to obtain the wire-bonding without delamination.

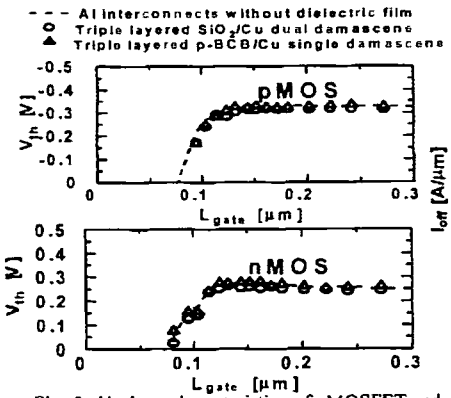


Fig. 5 V_{th}-L_{gate} characteristics of nMOSFET and pMOSFET with uncovered single Al interconnects, the triple-layered SiO2/Cu dual damascene interconnects and the triple-layered p-BCB/Cu SDIs interconnects with Cu-VPs.

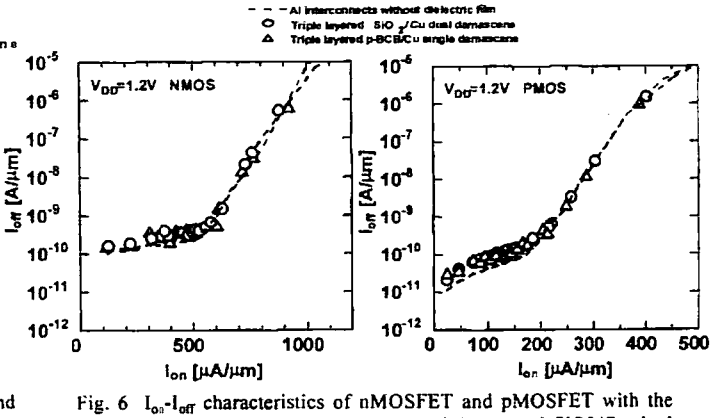


Fig. 6 I_{on}-I_{off} characteristics of nMOSFET and pMOSFET with the uncovered single Al interconnects, the triple-layered SiO2/Cu dual damascene interconnects and the triple-layered p-BCB/Cu SDIs interconnects with Cu-VPs. No special process damage is found during the triple-layered, Cu-SDI integration.

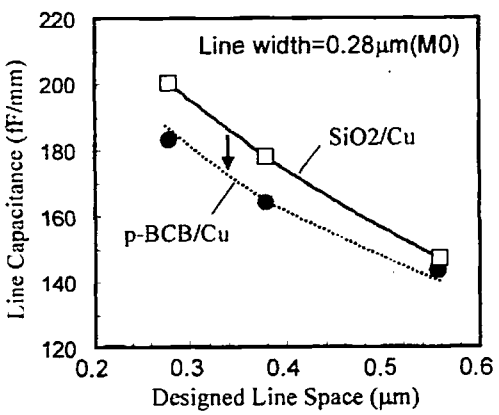


Fig. 7 Interconnect capacitance as a function of line space for the lowest level lines (M0) of the p-BCB/Cu and the p-CVD SiO2/Cu.

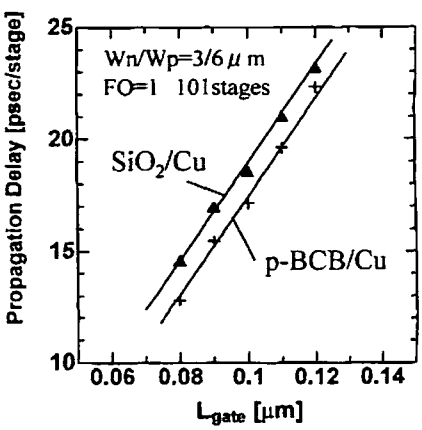


Fig. 8 Propagation delay as a function of the gate length for the CMOS ring oscillators after full interconnect integrations of the triple-layered p-BCB/Cu-SDI, and of the conventional triple-layered SiO_2/Cu dual damascene interconnects.

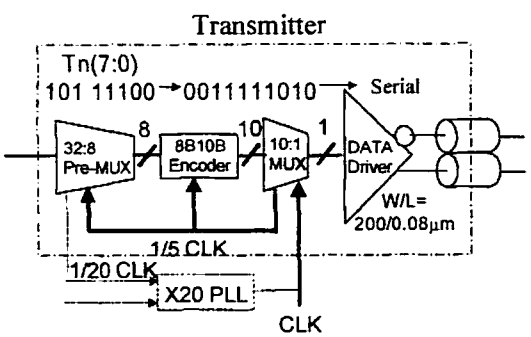


Fig. 9 Block diagram of CMOS transmitter with triple-layered interconnects, in which the 8bit signal from 32:8 pre-MUX is transformed, through 10bit signal by 8B10B encoder, to 1bit serial signal by 10:1 multiplexer (MUX).

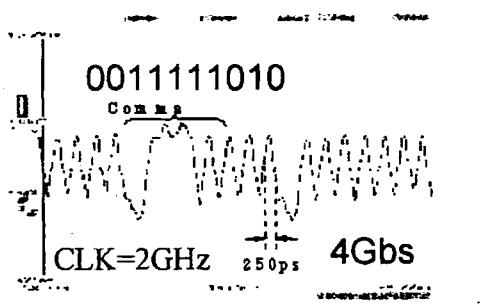


Fig. 10 Measured waveforms of 4Gb/s serial signals by 0.08μm CMOS transmitter with the triple layered p-BCB/Cu SDIs.