Performance of 100-kV advanced nanoelecron-beam Exposure system, JBX-9300FS, and its application of sub-100-nm CMOS devices

Yukinori Ochiai, Takashi Ogura,
Mitsuru Narihiro, H. Arai and Tohru Mogami

Silicon Systems Research Laboratories,
NEC Corporation, Japan

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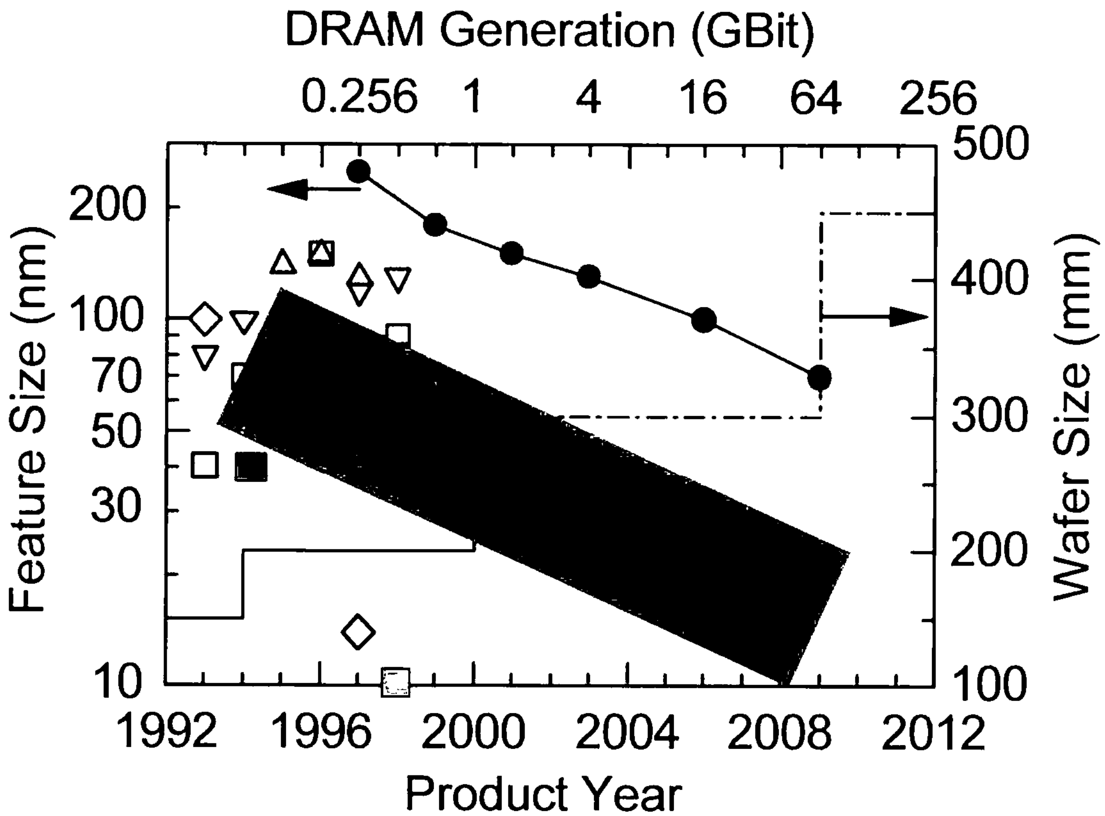
outline

1. Introduction
2. Specifications of JBX9300FS
4. Exposure performance
5. Wafer mark detection
6. Mix and Match lithography
6. Summary

Device miniaturization



Feature size and wafer size trends according to SIA road map and various institute

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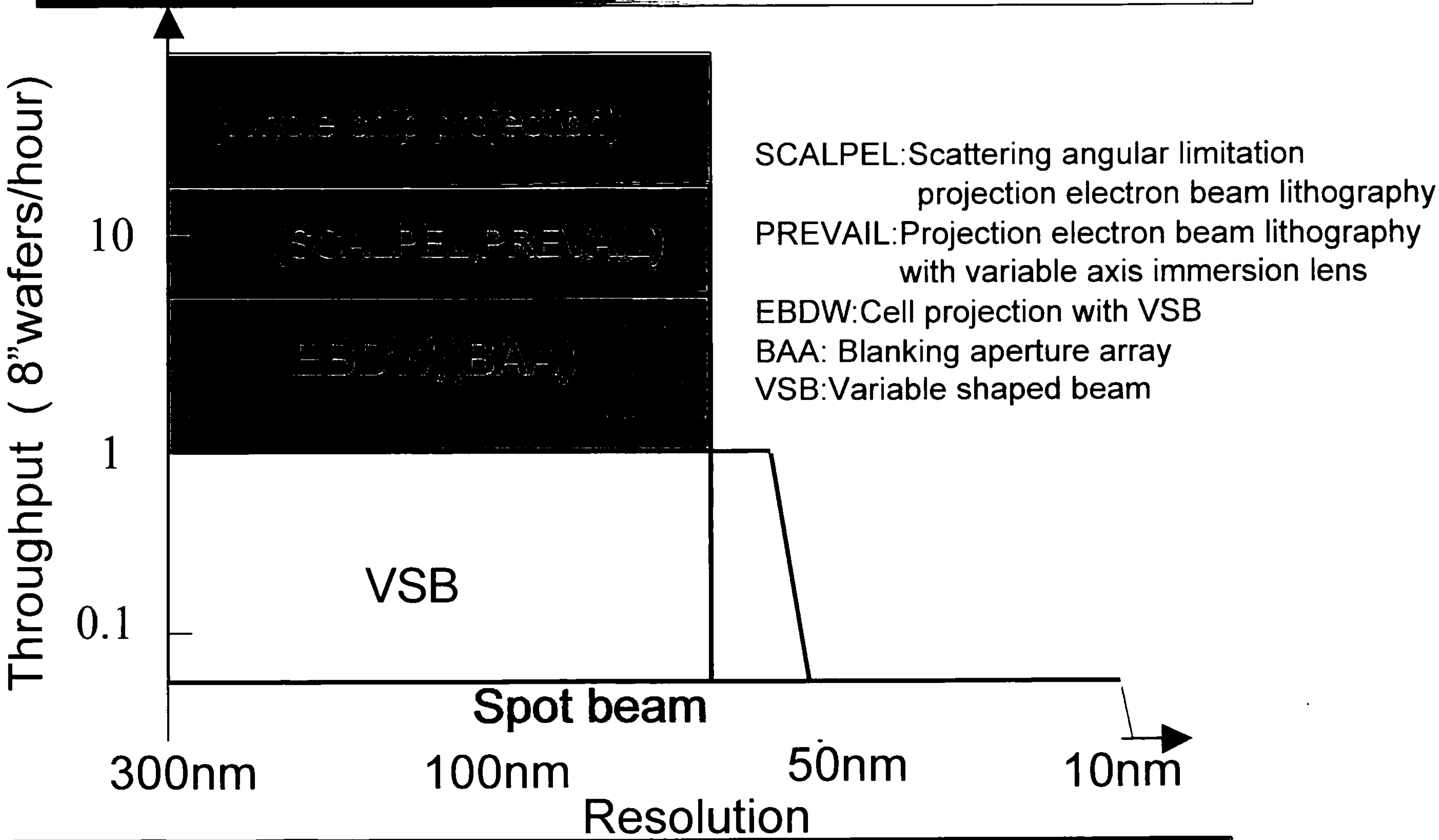
Throughput for various types of Electron beam exposure



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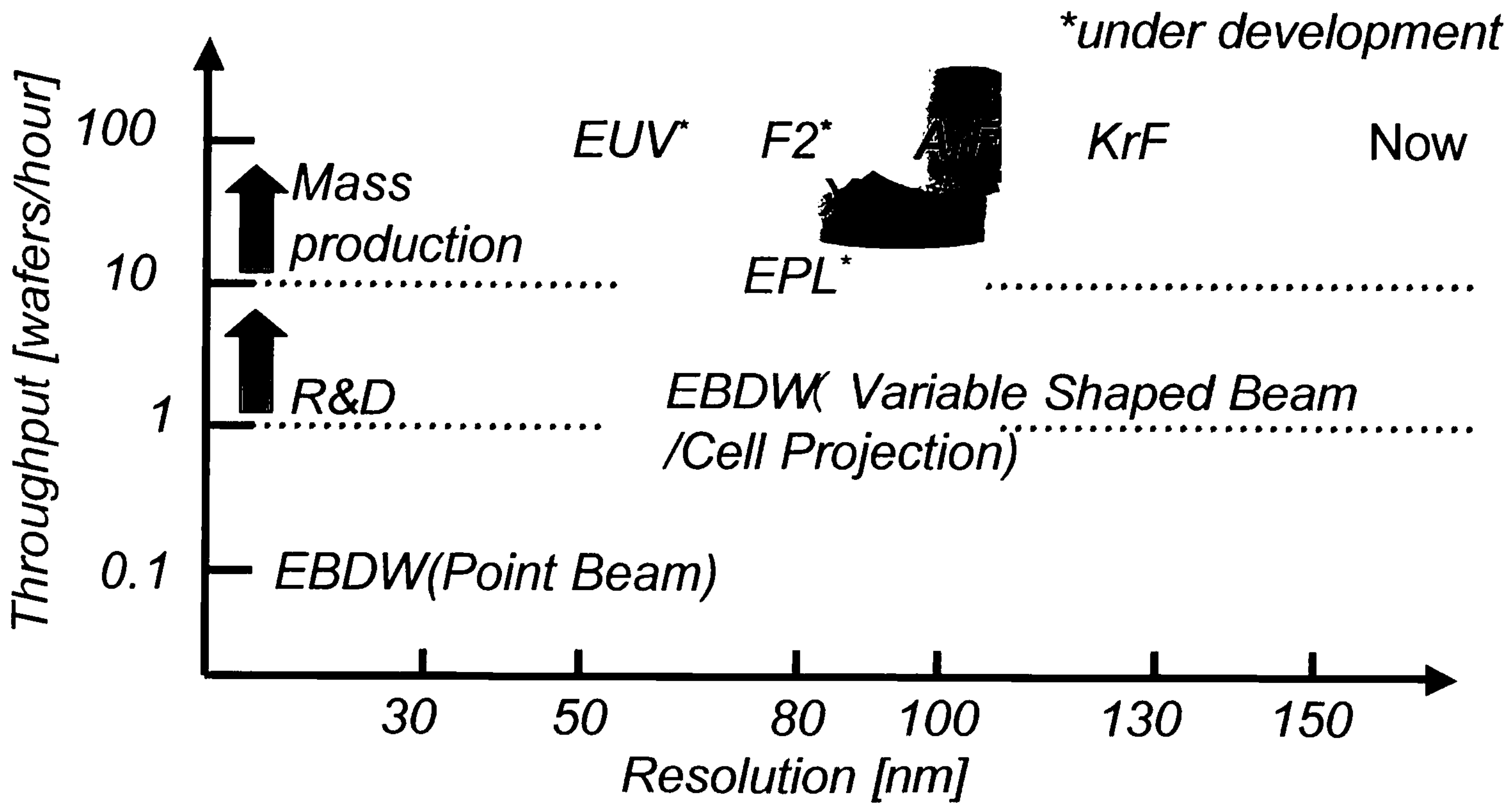
Lithography Techniques

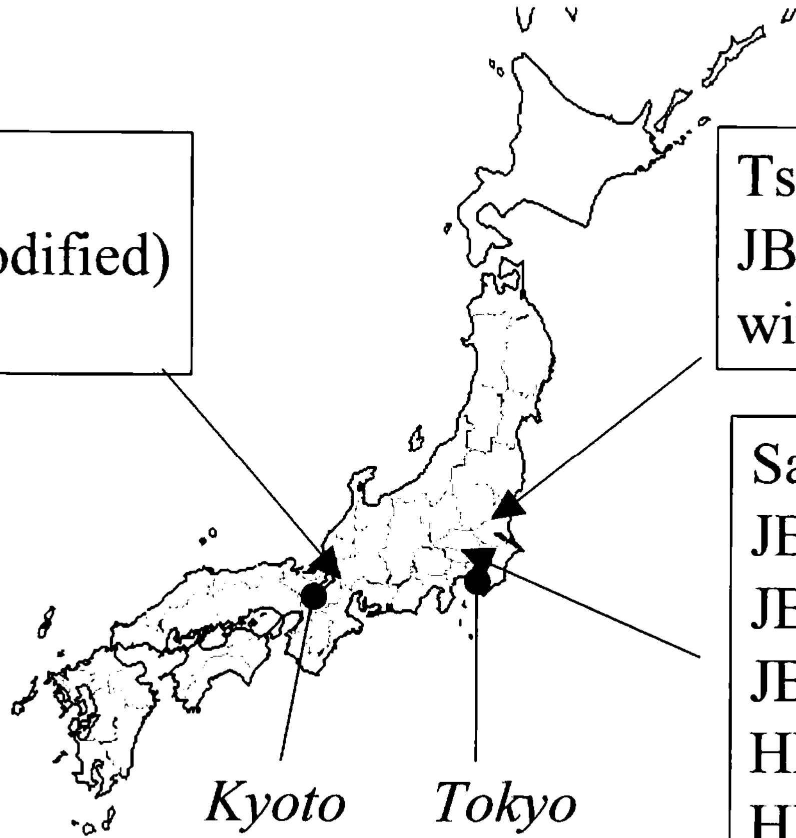


Background

EB systems used in NEC, *Japan*

Ohtsu:
JBX-5D Ⅱ (modified)
JBX-6000FS

Tsukuba:
JBX-5FE
with 12MHz DAC



Sagamihara:
JBX-9300FS
JBX-9000MV
JBX-7000MV
HL-800D
HL-900DX
MEBES

Aim and requirements of our EB system in Sagamihara, NEC

Research and development sub-100nm advanced CMOS

1.Wafer size

- 12-inch (maximum) wafer available stage.
- X-ray mask available

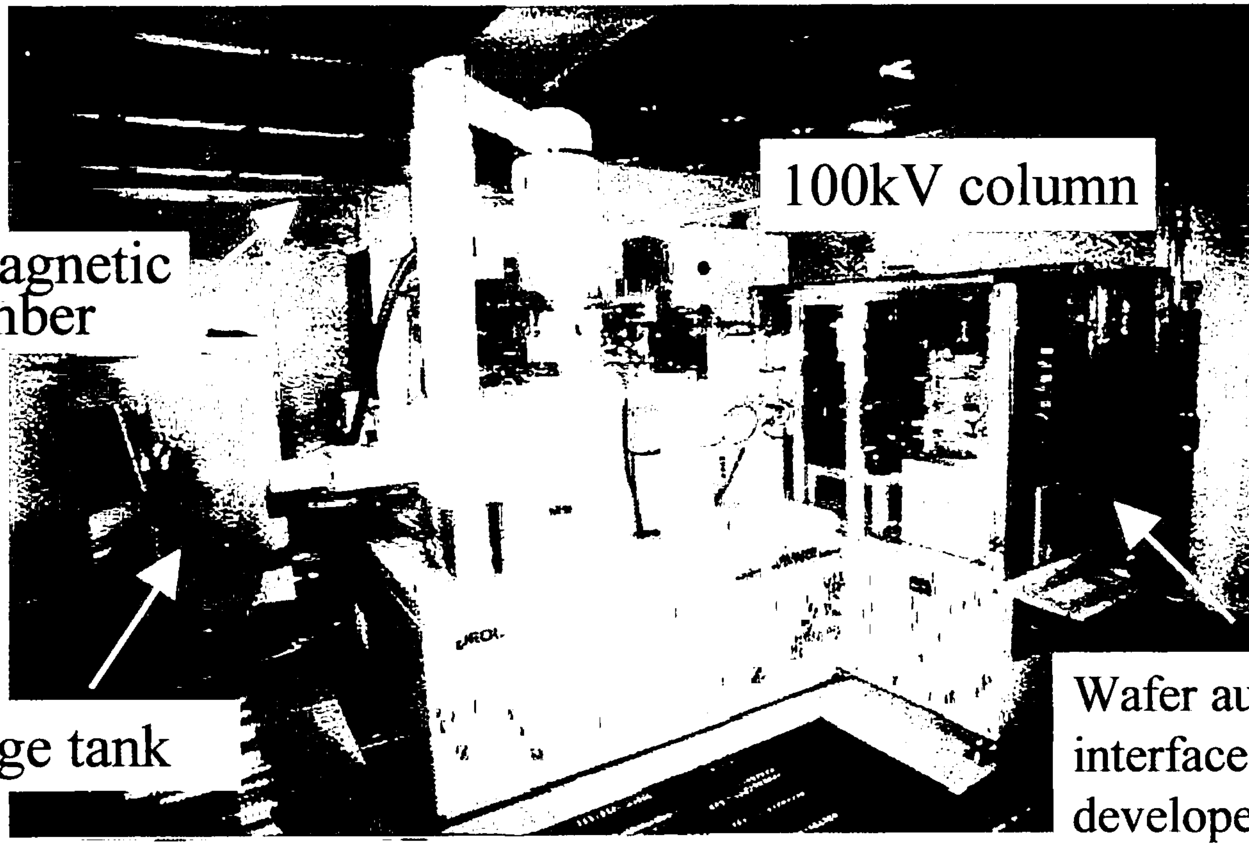
2.High-throughput

- high-frequency deflection
- large field
- in-line developer

3.High-precision lithography

- high-acceleration energy(100kV)
- dynamic focus and dynamic stigma correction with wafer-height measurement
- wafer mark detection with self-correlation method

JBX-9300FS installed in NEC Sagamihara



JBX-9300FS with automatic developer is installed in a thermal shield.

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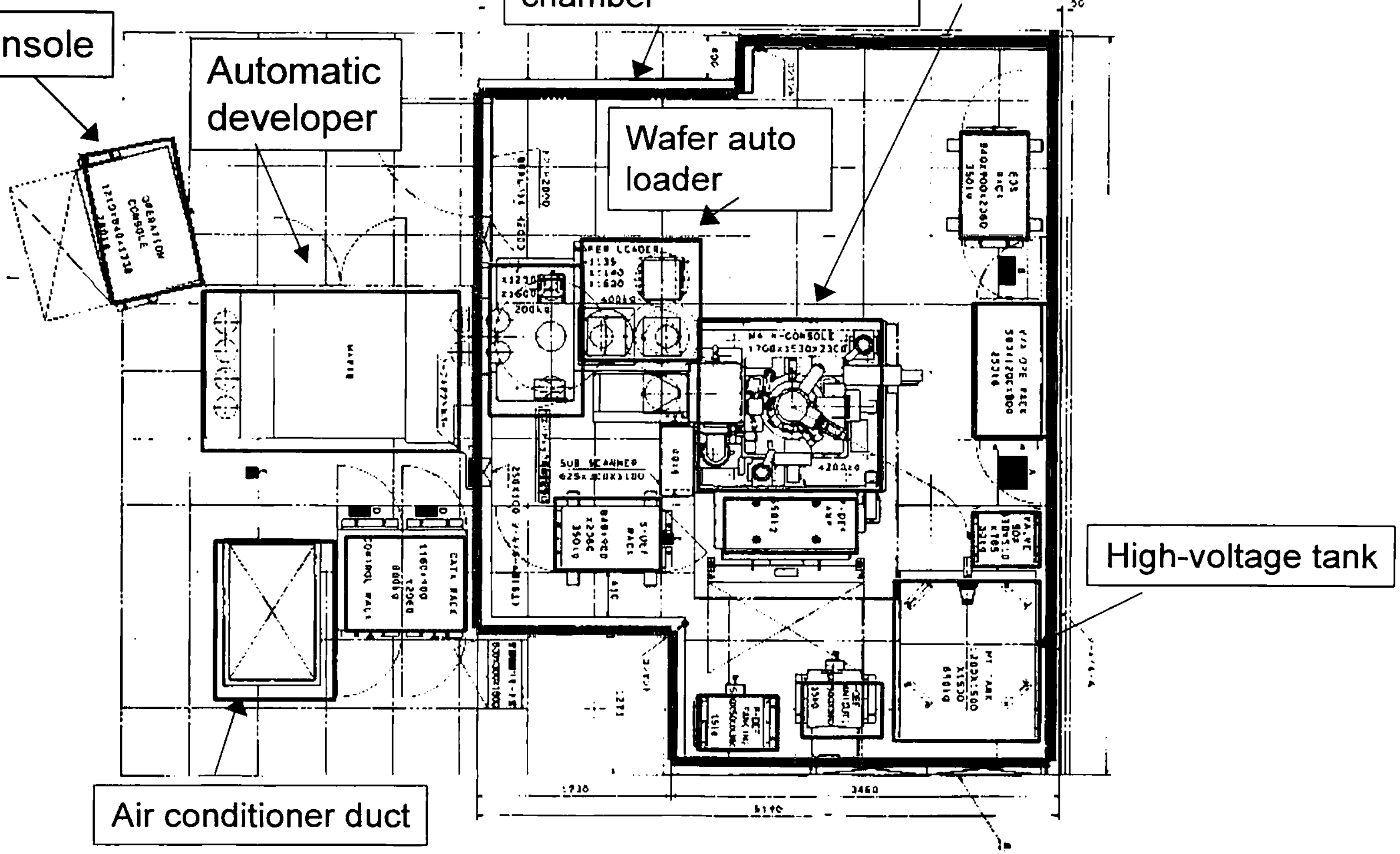
Progress in introduction of JBX-9300FS at NEC

Dec 1997 start to construction of floor reinforcement
and thermal magnetic shield chamber
May 1998 carry in and installation of JBX-9300FS
Aug 1998 first beam at 50 kV

May 1999 finish of installation at 50 kV

June 2000 finish of installation at 100 kV

EB system arrangement



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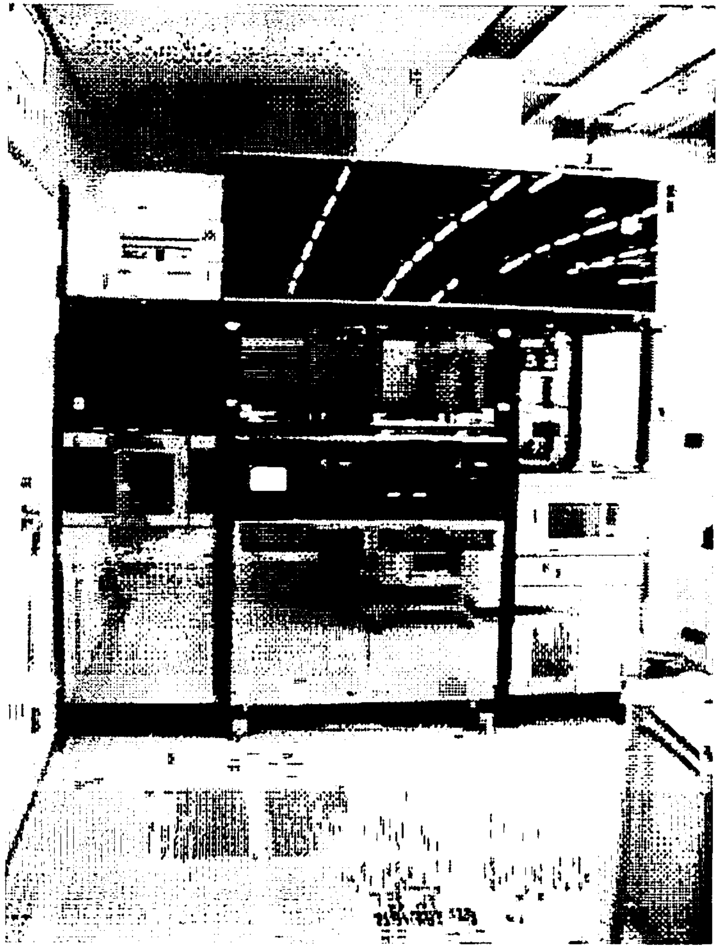
Automatic developer for 8-inch wafer



- >50 wafers/hour
- developer:TMAH/organic
- chemical filter installed

Mark 8 made by TEL
(Tokyo Electron Ltd.)

Specifications of EB system 1

beam type	:spot beam
electron source	:ZrO / W TFE
Acceleration voltage	:50 / 100kV
Scanning	: vector scan
stage movement	: step & repeat
wafer size	:6, 8, 12inch,X-ray mask
resolution of laser interferometer	:0.62nm
main deflector DAC	:20 bit
dynamic focus and stigma correction with wafer height measurement	:height measurement accuracy 0.1μm

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Specifications of EB system 2

Deflection:	: 1- and 2-stage available 1-stage for high precision 2-stage for high frequency deflection
Deflection speed:	: >25MHz
Field size:	: 1000μm × 1000μm at 50 kV 500μm × 500μm at 100 kV
Sub field:	: 10μm × 10μm at 50 kV 5μm × 5μm at 100 kV
Beam deflection step	: 2nm at 50 kV 1nm at 100 kV
Thermal magnetic shield chamber	: controlled at ±0.1°C
in-line automatic developer	: for 8 inch wafer

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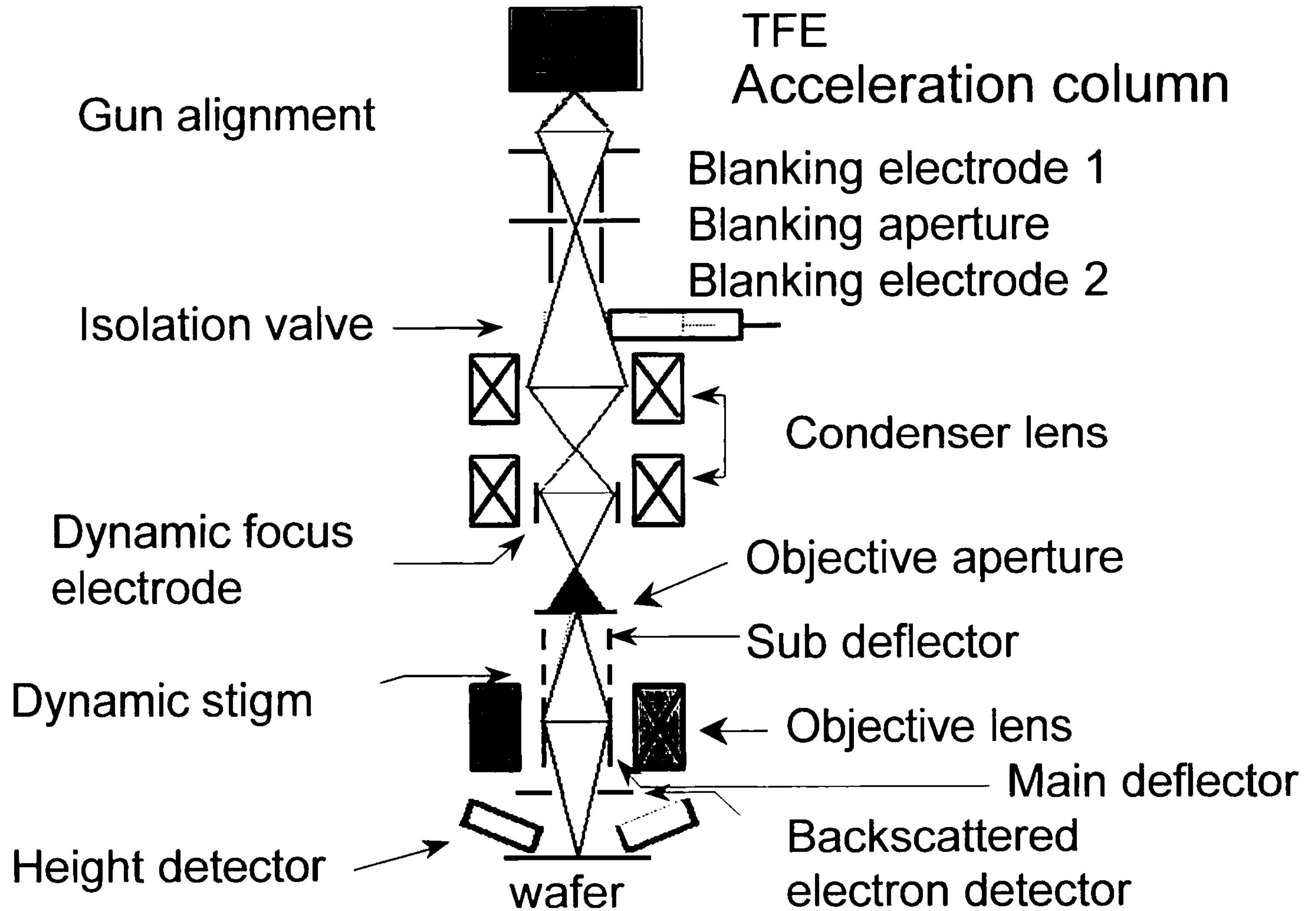
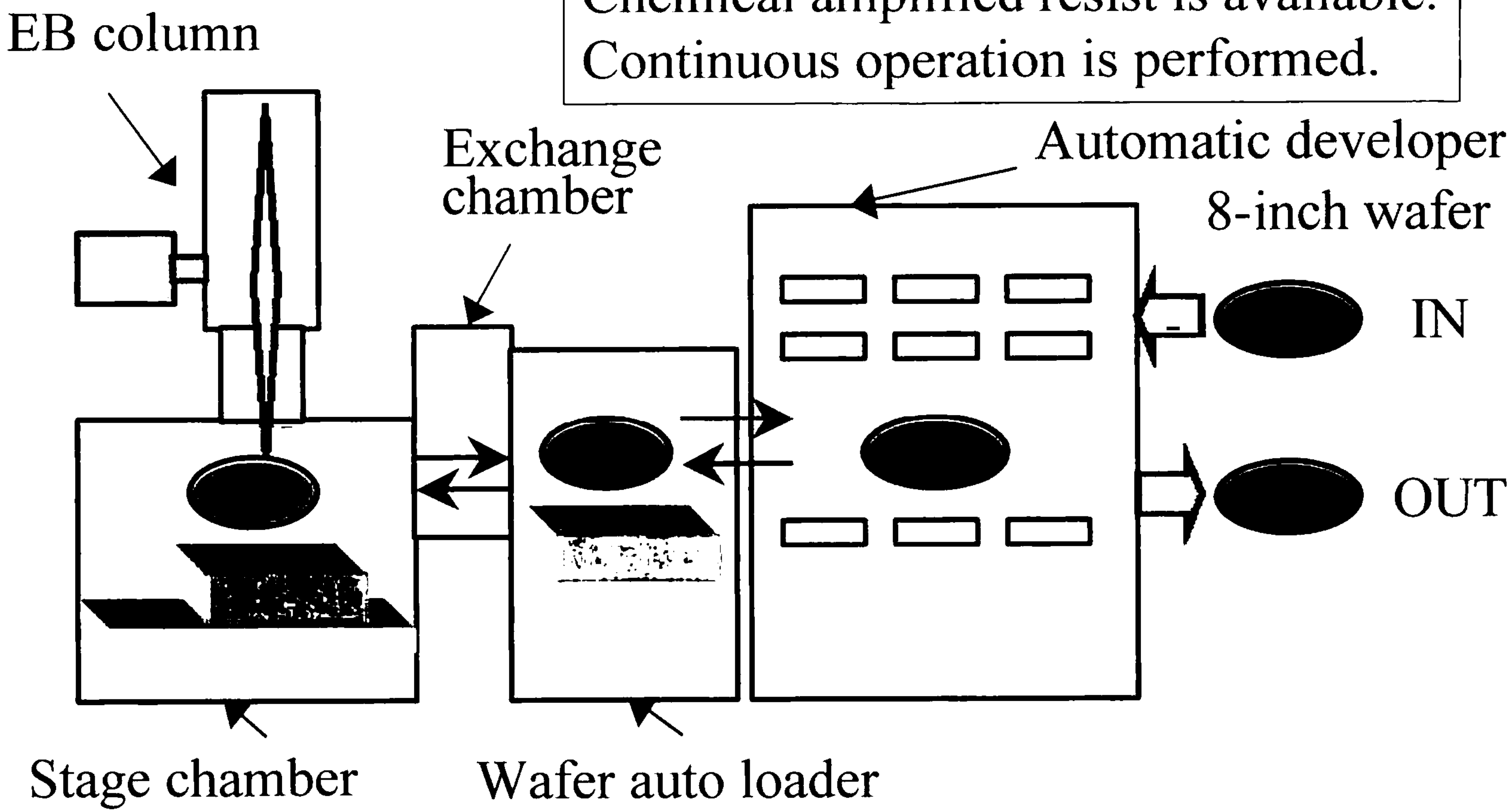
Electron optical column



Inline developer for 8-inch wafer with EB exposure

Chemical amplified resist is available.
Continuous operation is performed.



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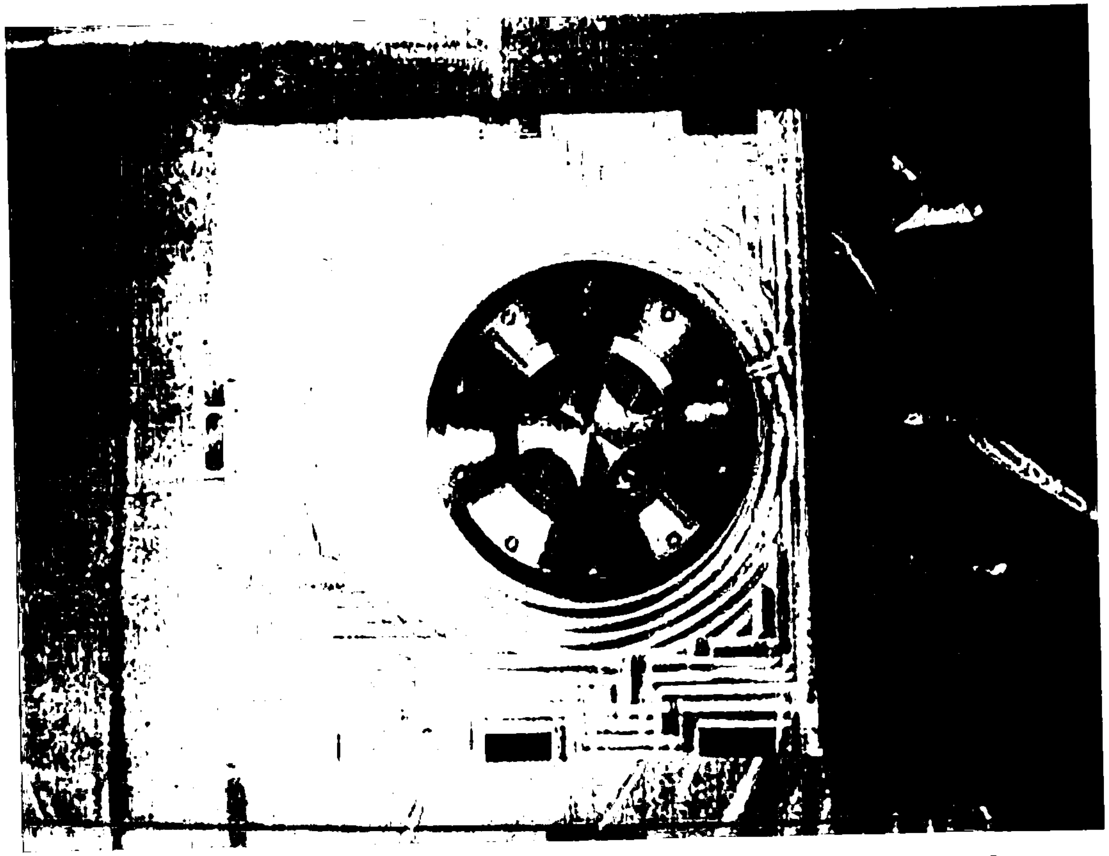
X-ray mask cassette



For NIST specified X-ray mask

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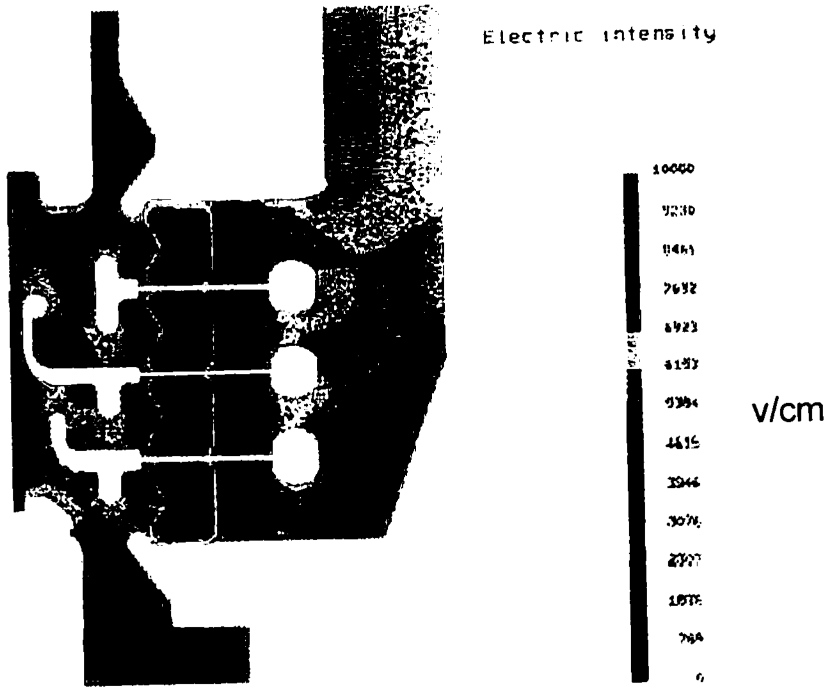
4-stage accelerator



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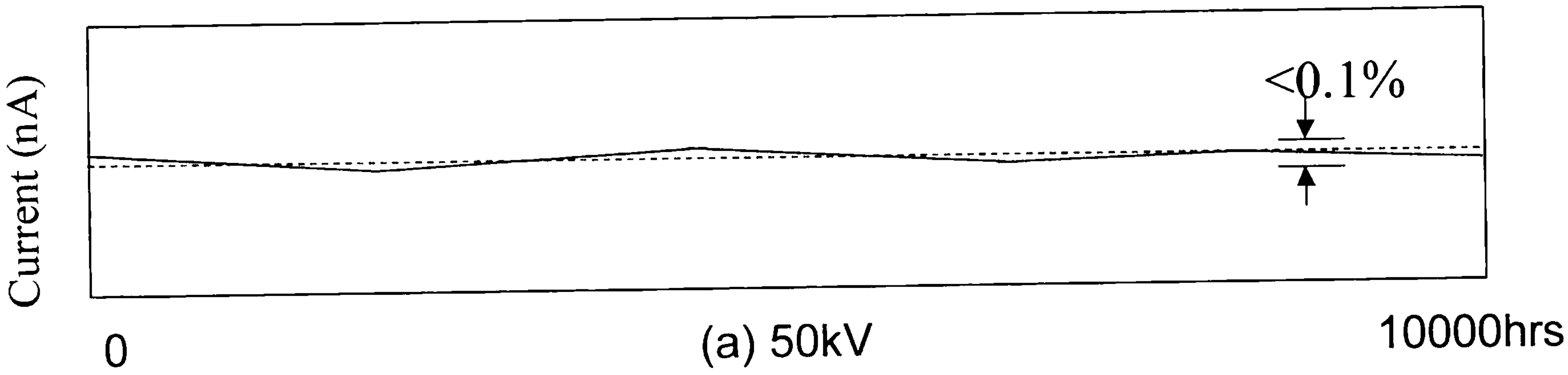
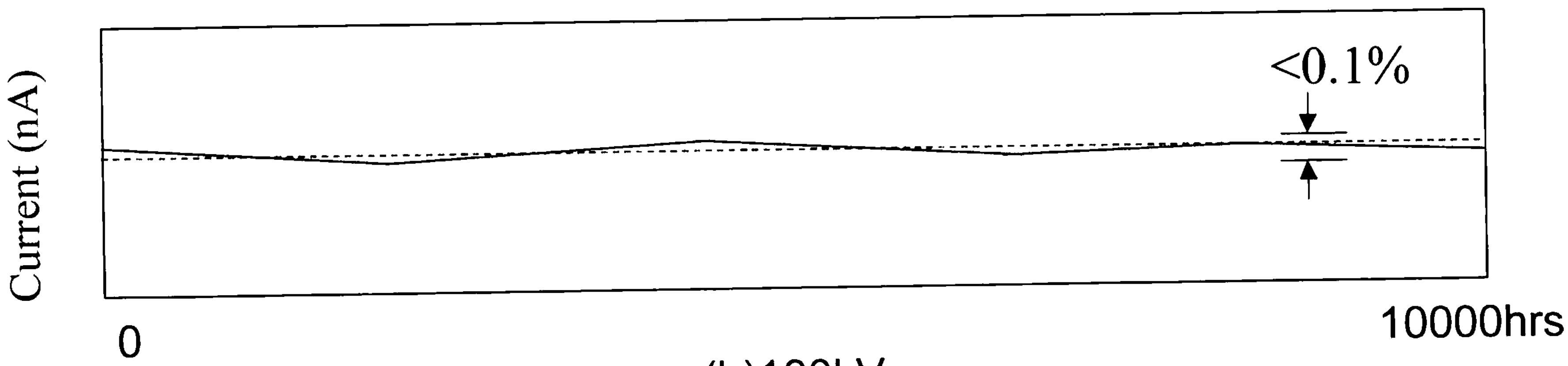
Beam stability at 50 and 100kV



(a) 50kV



(b)100kV

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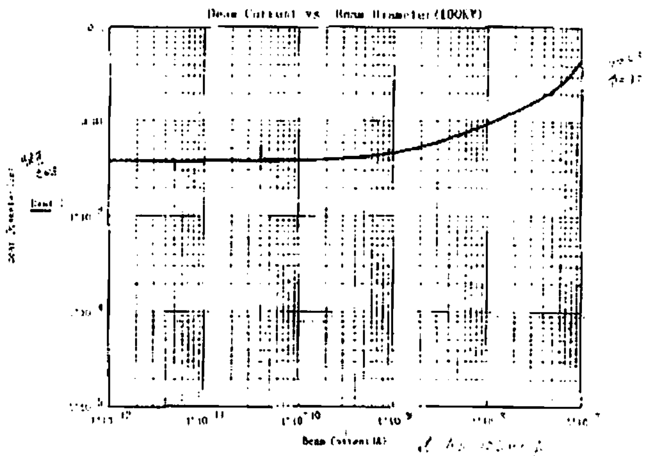
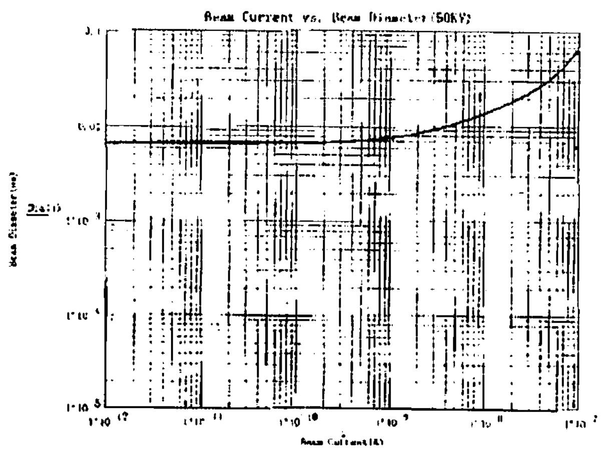
Electron beam diameter dependence on beam current



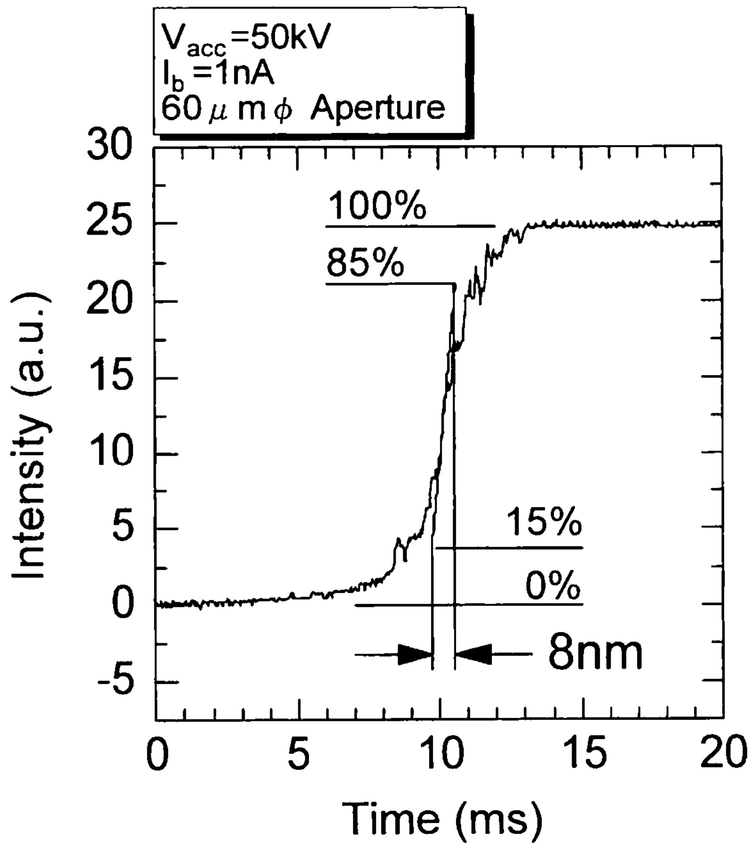
100kV



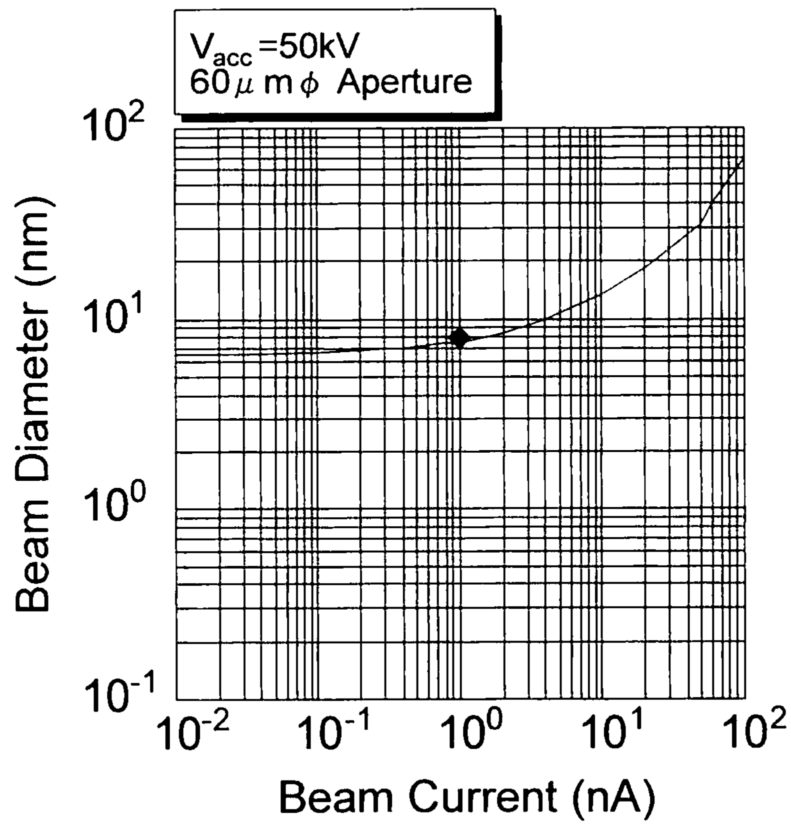
50kV

Calculation results

Beam diameter measurement



(a) knife edge method(50kV、1nA)



(b) beam diameter(calculation)

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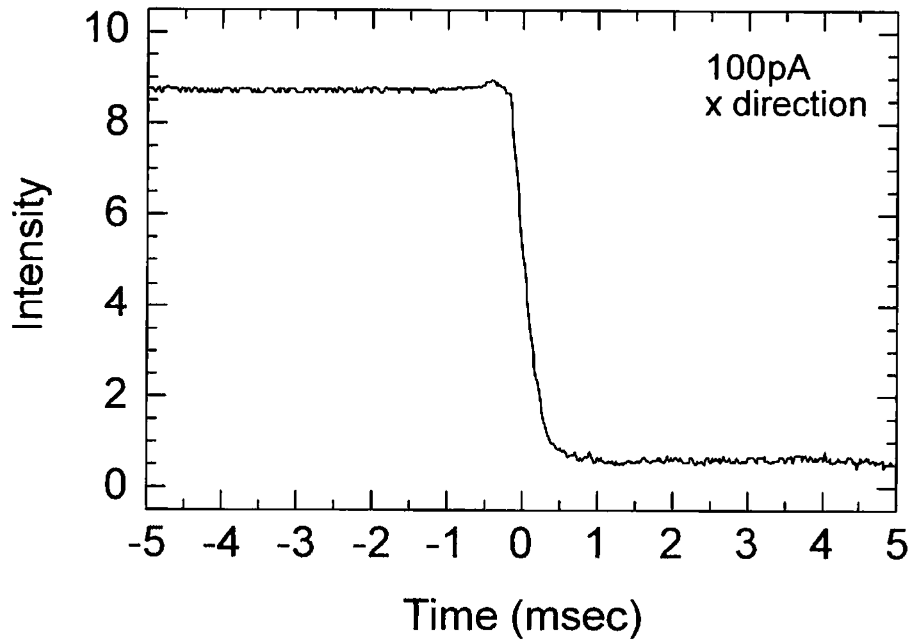
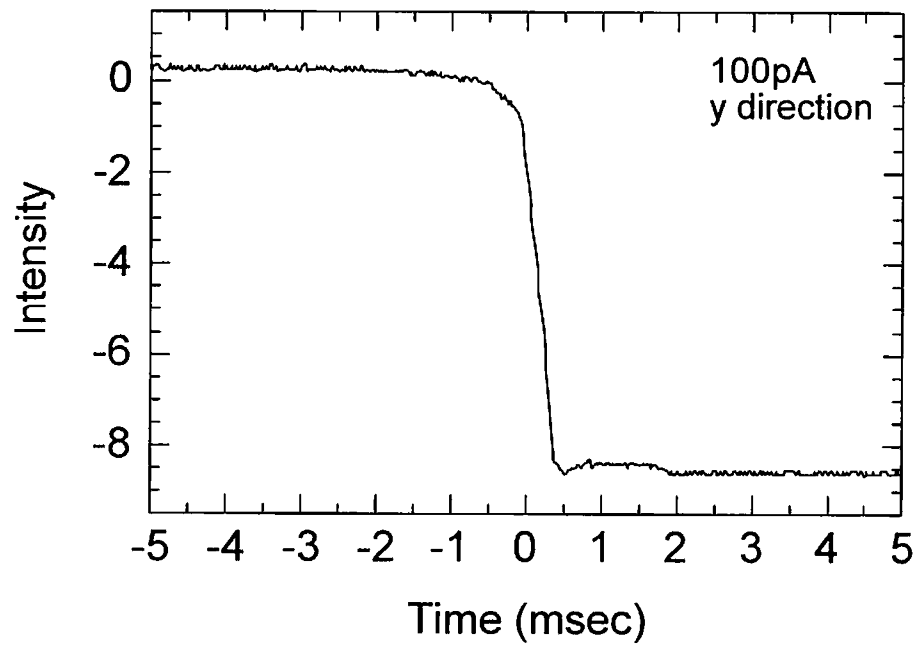
Beam diameter measurement at 100 kV



dx=3.6nm



dy=4.0nm

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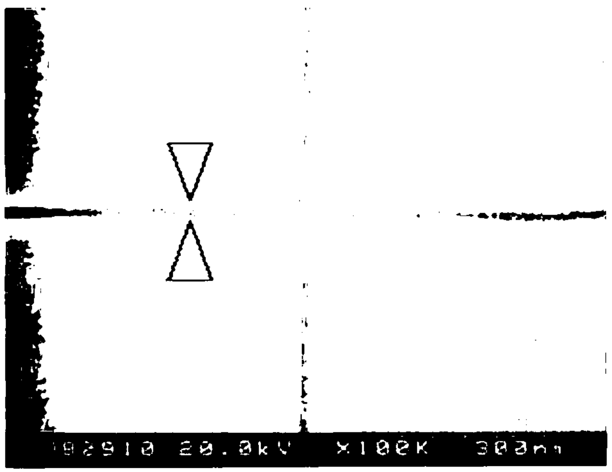
Exposure performance

resist: ZEP520(positive resist)、
thickness: 30nm、 developer: amyl acetate
V_{acc}=50kV、 I_b=100pA、 420mC/cm^2、
2stage deflector

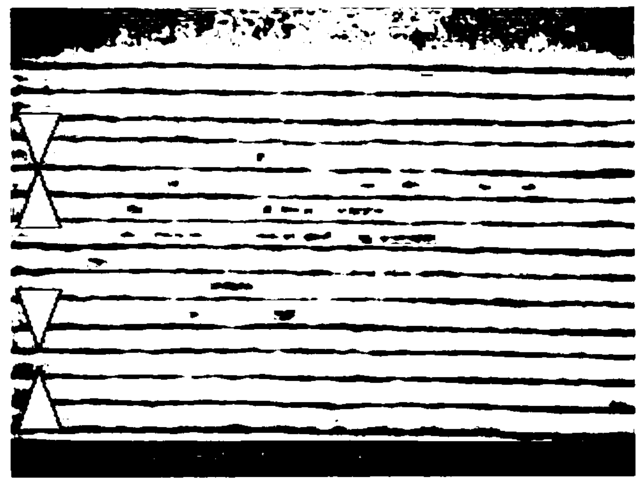
Width:
25nm



(a) cross pattern

width:
13nm

period:
50nm



(b) L/S pattern

30-nm width negative resist pattern with 265-nm height

EB: 50kV 200pA (JBX-9300FS)
Resist: NEV22A3 chemically amplified resist
(Sumitomo Chemical Co.)
Standard sensitivity: 9.5 $\mu C/cm^2$
Wafer: polysilicon/8-inch silicon
PB 110°C for 60sec
with proximity effect correction
(α=15nm, β=10mm, γ=2.9)
with Dynamic focus/Dynamic stigma
scanning field: 1 mm with Height Correction.
PEB 100°C for 60sec
Development: TMAH 2.38% for 60s

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100-nm diameter positive resist pattern with 600-nm height

EB: 50kV 200pA (JBX-9300FS)
Resist: UV5 chemically amplified resist
(Shipley Co.)
Exposure dose: 28 $\mu C/cm^2$
Wafer: 8-inch silicon
PB 110°C for 60sec
with Dynamic focus/Dynamic stigma
scanning field: 1 mm with Height Correction.
PEB 145°C for 75sec
Development: TMAH 2.38% for 45s

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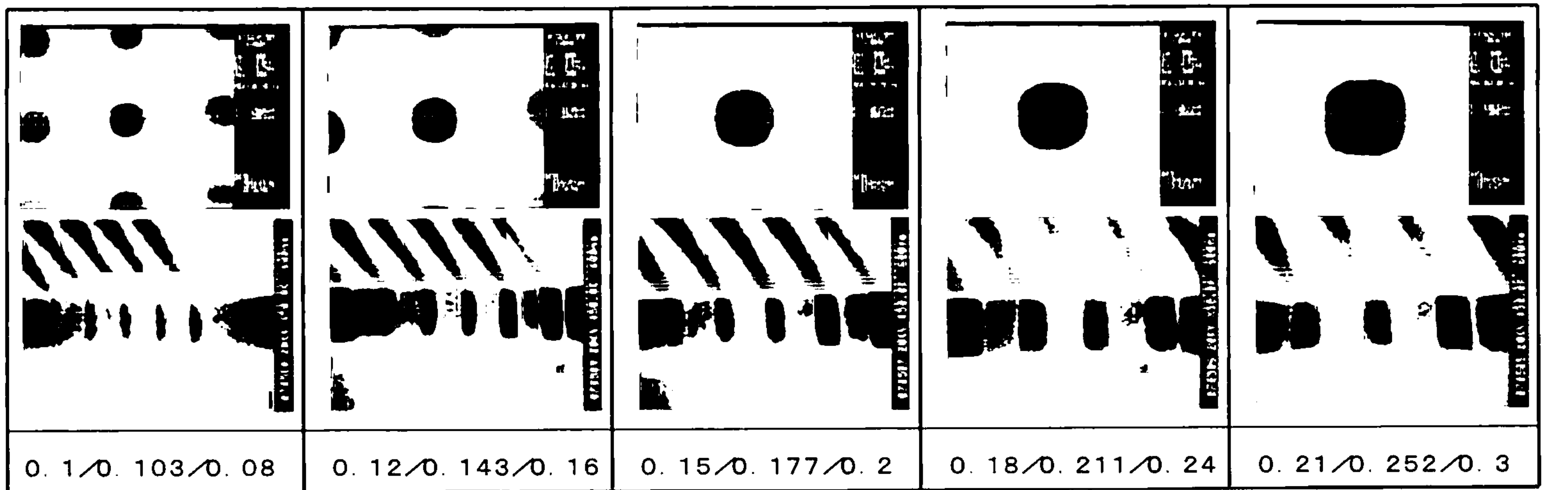
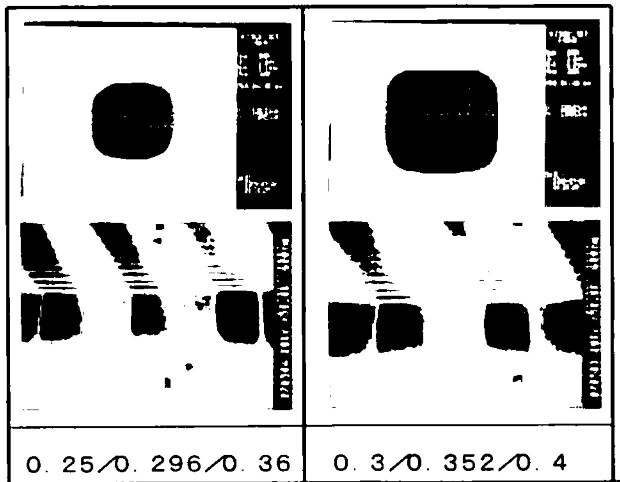
Contact hole exposure at a dose of 28 μC/cm on UV-5 resist





designed／by CD-SEM／cross-sectional SEM (μm)
Designed patterns ares rectangle.

Resist UV-5 0.6 um thickness

EB 50 kV, 196 pA,
beam step 2x6=12 nm
Dose 28 uC/cm2
Proximity correction: none

Development PEB 145 C, 75 sec
Developper TMAH(2.38%), 45 sec

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0.09 μm L&S pattern for wiring (positive resist) at 50 kV

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Wafer mark detection

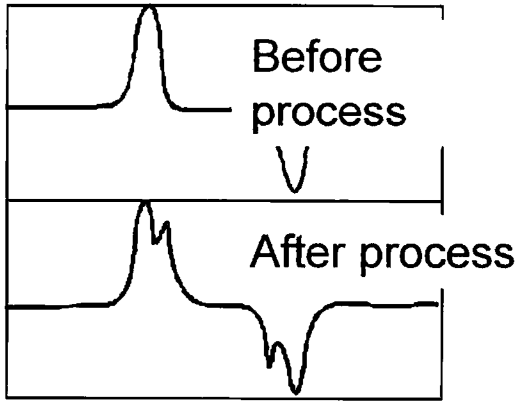
Requirement for wafer mark detection

- high mark detection accuracy for high-overlay accuracy
- apply for CMOS LSI gate, contact, and wiring lithography

Problem

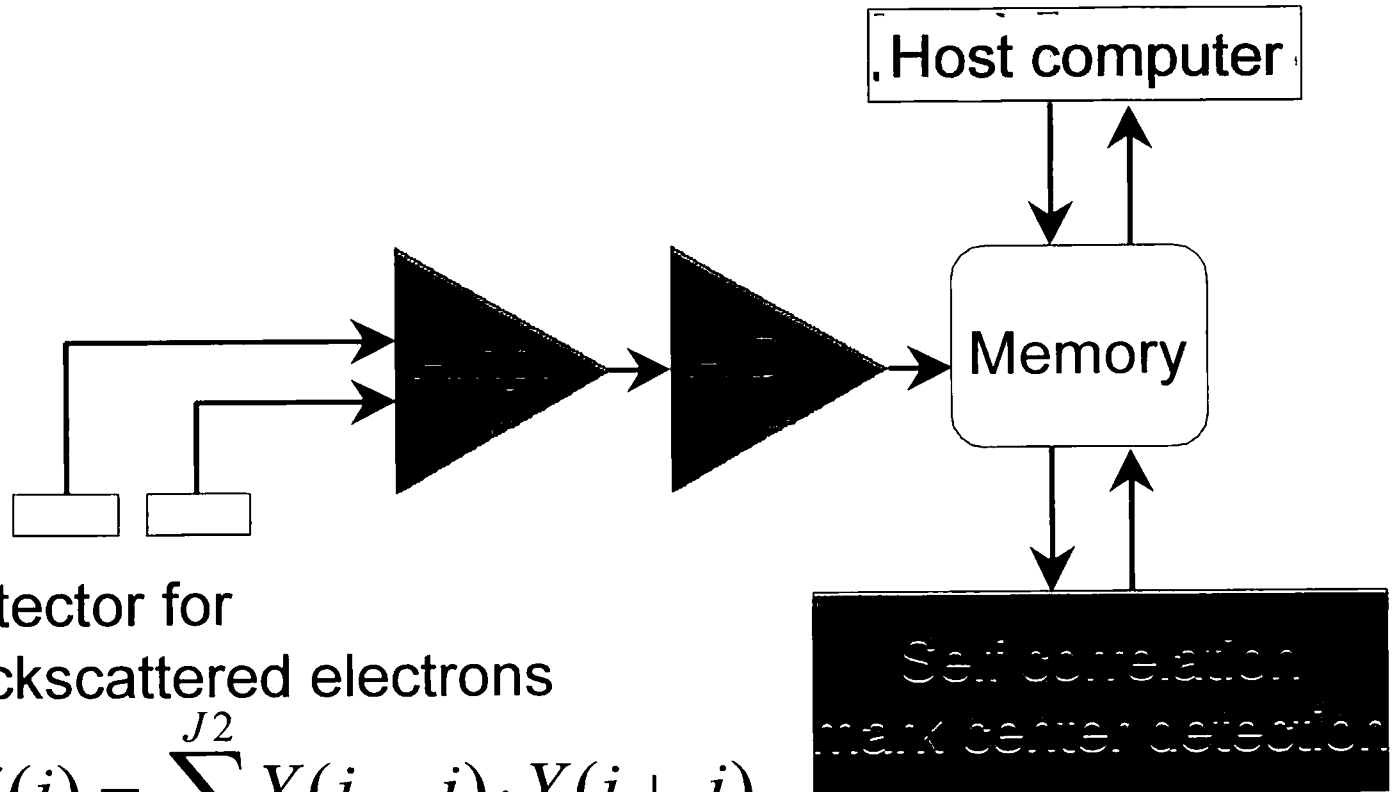
- mark damage due to device process

Degradation of S / N on mark signal
Modification of mark signal



Accumulation of mark detection signal and self-correlation method

Mark detection using accumulation and self correlation method



$$Z(i) = \sum_{J=j1}^{J2} Y(i-j)\cdot Y(i+j)$$

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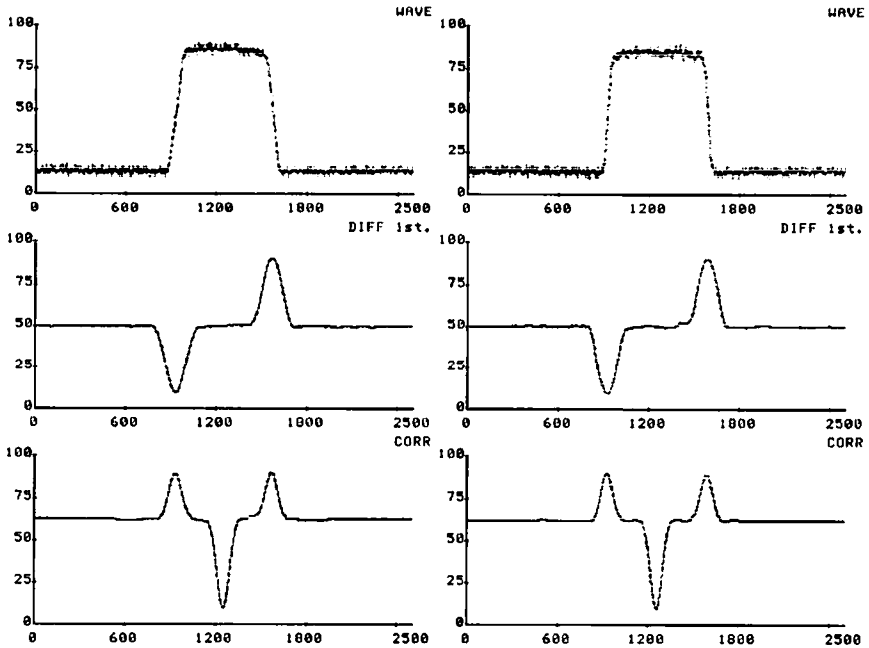
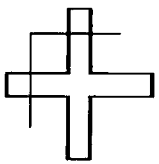
Mark detection of Au-metal-cross mark

X- direction

Y- direction





accumulation
(50times)

deferential

self-correlation

Mark detection signal (V_{acc}=50kV、I_b=100pA)

Mark detection repeatability: $2\sigma_x$=5.2nm、$2\sigma_y$=5.4nm

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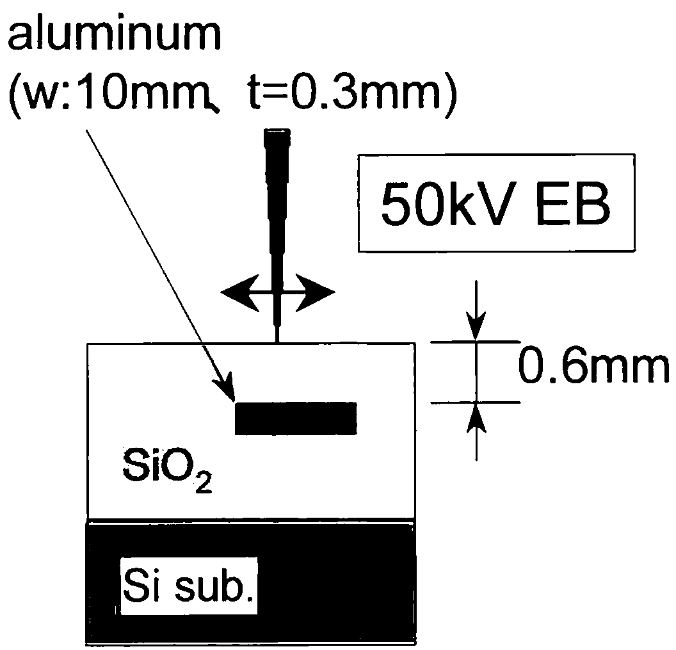
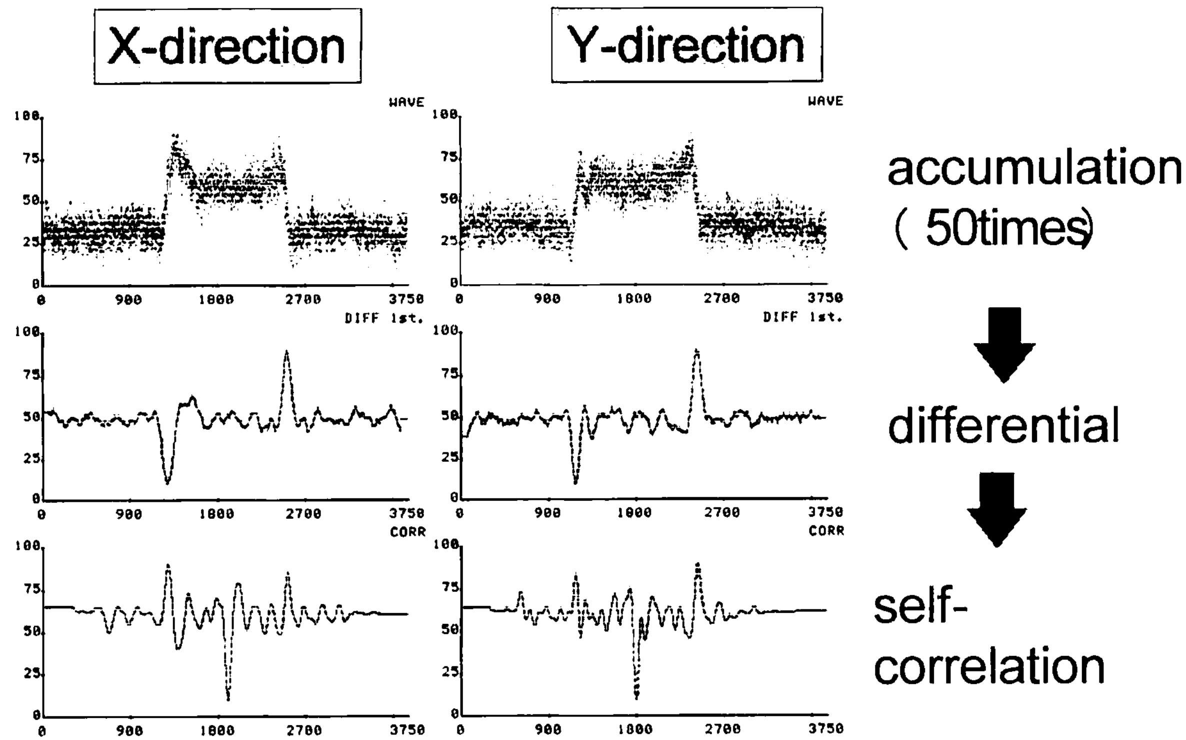
Mark detection accuracy by using device pattern



(a) cross section of mark sample



(b) mark detection signal (V_{acc}=50kV, I_b=2nA)

Mark detection repeatability: $2\sigma_x$=25.0nm, $2\sigma_y$=24.0nm

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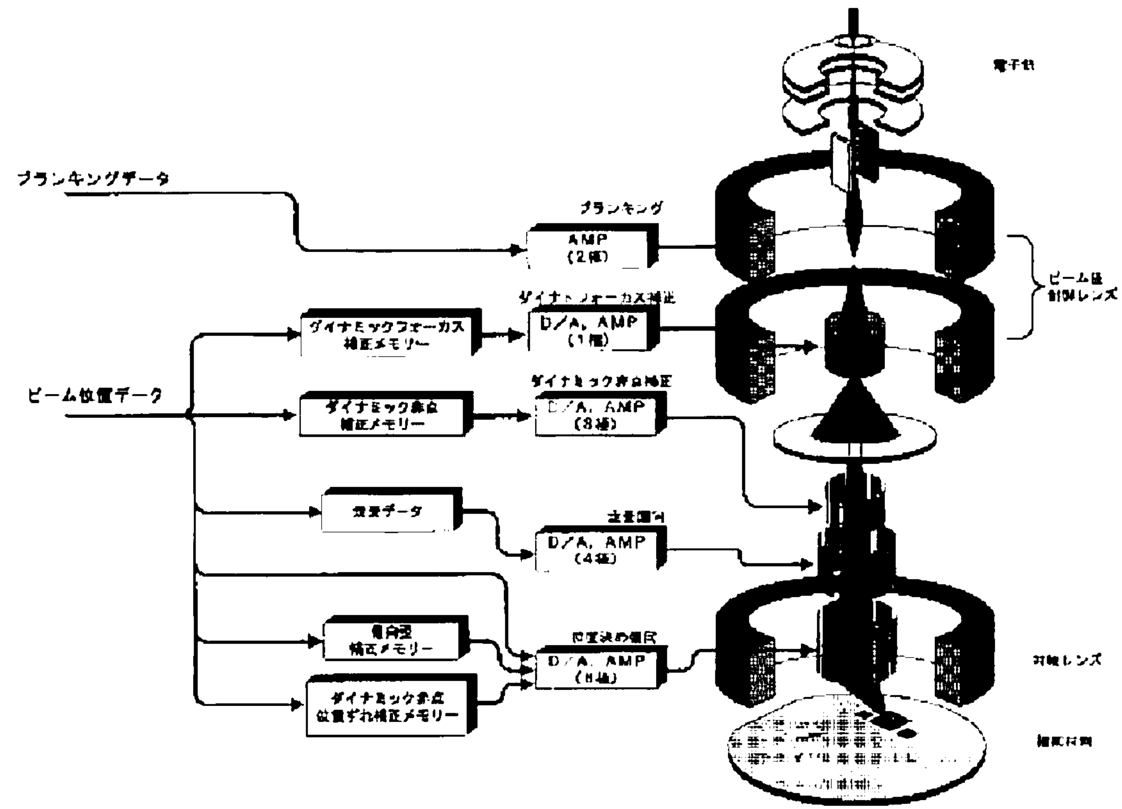
Beam control



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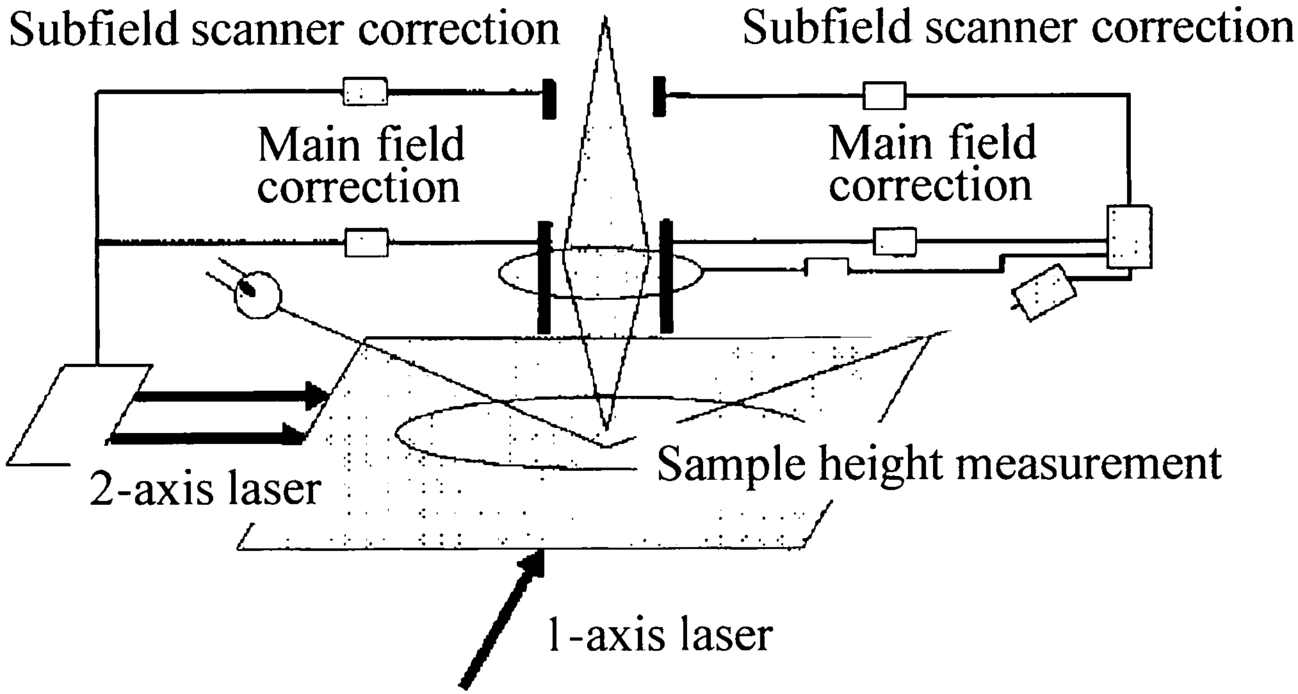
Beam position and focus correction system



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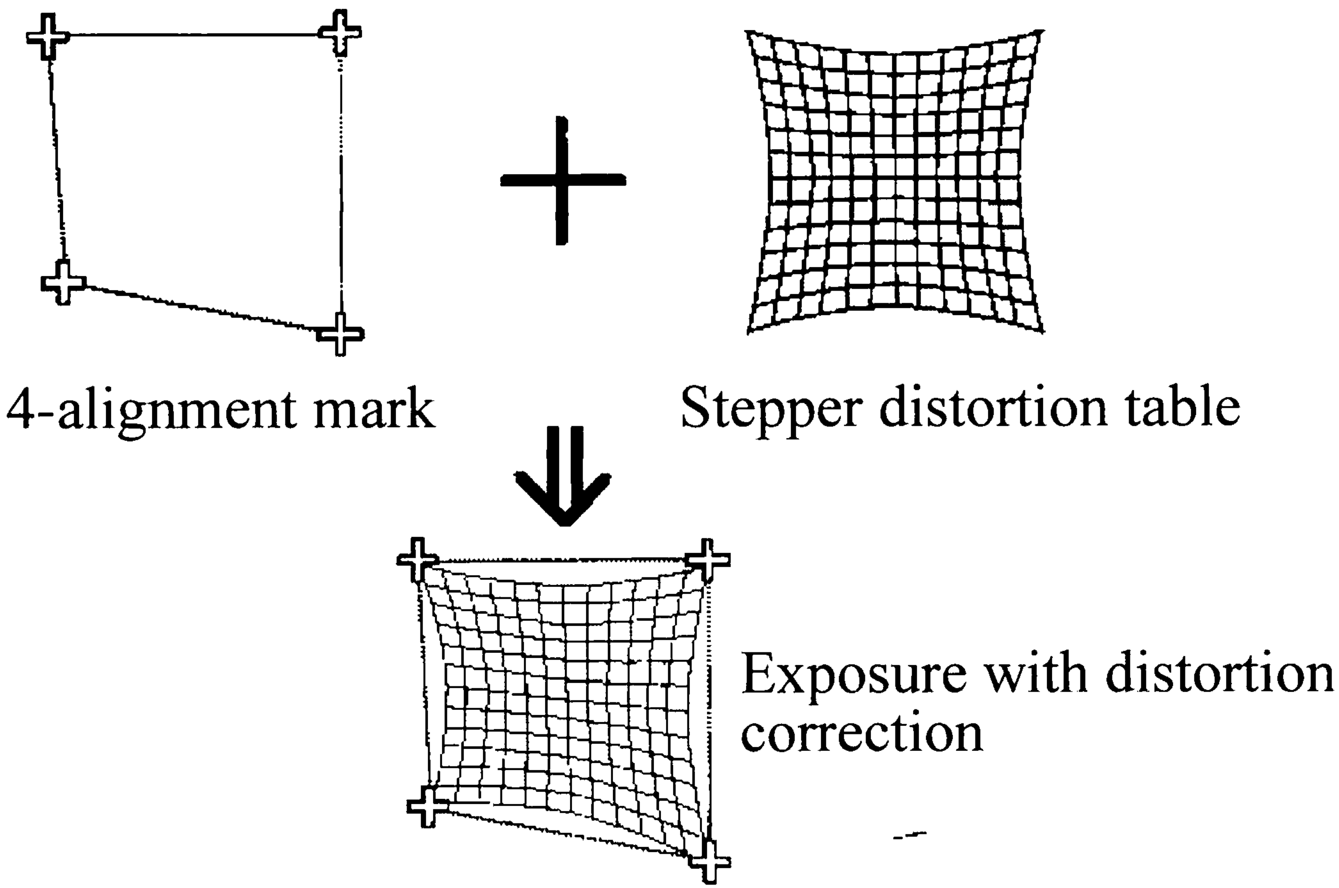
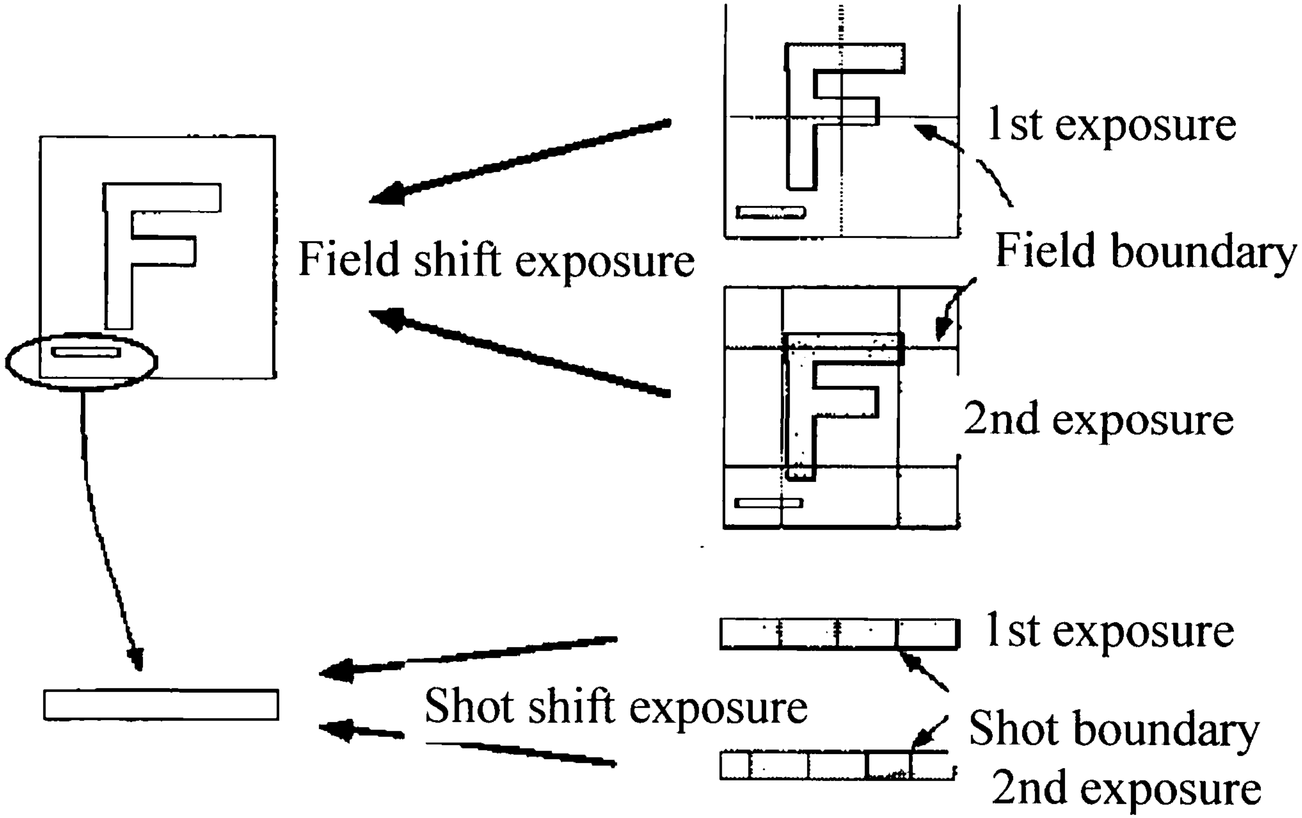
Overlay exposure



Field shift and shot shift exposure



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