Lithographic Performance and Mix-and-Match Lithography Using 100 kV Electron Beam System JBX-9300FS

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We evaluated the performance of 100-kV point electron-beam lithography system: JBX-9300FS and developed Mix-and-Match lithography process. Resolution on resist exposure is 30-nm using commercially available chemically amplified resist and is down to 10-nm-order using Calixarene resist. For high-throughput lithography, Mix-and-Match lithography process was developed including pattern preparation, and EB exposure time decreased to 1/3. These process technologies are useful for development of advanced CMOS devices.

Introduction

Recently, for the increase in the performance of logic devices, the feature size of CMOS devices is rapidly decreasing less than 100 nm as predicted by ITRS 1999 (International Technology Roadmap for Semiconductors). [1] Lithography technology is the key to realize sub-100-nm high-performance devices, then several types of high-throughput lithography tools are under development such as F_2 excimer laser lithography, EUV (Extremely Ultra Violet) lithography and EPL (Electron Projection Lithography). On the other hand, advanced CMOS devices with a gate length of less than 100 nm should be also developed ahead of mass production. For this purpose, high-resolution point electron beam lithography is only a tool for the research and development of devices on a full wafer.

We have introduced an advanced point electron beam system, JBX-9300FS, which is designed for the development of advanced devices with a small feature size on a large silicon wafer. In this report, the performance of JBX-9300FS on lithography and development of Mix-and-Match lithography are described.

Lithographic Performance

Figure 1 shows a photograph of the first EB column installed at NEC Sagamihara plant. [2] Recently the size of silicon wafers increases with increasing chip size and device density, so that high productivity is obtained and production cost decreases. Currently, 8-inch wafers are used in both R&D and mass production, but 12-inch wafers are being introduced to the semiconductor industry. Research in sub-0.1-μm device continues intensively. In order to obtain high throughput, chemically amplified resists are commonly used in both optical and electron beam lithography. Therefore, it is necessary that a high-resolution electron-beam lithography system can handle a chemically amplified resist and large wafers for next generation process. JBX-9300FS has several advanced or new features to obtain high-resolution, high-accuracy and high-throughput for device development on large silicon wafers. [3] The electron column is operated at an acceleration voltage of 50 kV and 100 kV to obtain small beam diameter of 7 nm for 50 kV and 4 nm for 100 kV with a large deflection field of 1000 μm and 500 μm, respectively. Large deflection field contributes to obtaining high-throughput by reducing a number of stage motions. The maximum deflection clock is over 25 MHz. Dynamic focus and dynamic stigma correction are installed to obtain high-resolution and high-placement accuracy in a large field. An 8-inch wafer is available for full exposure and a 12-inch wafer is laudable. The system has an automatic wafer cassette loader, which can be used with an automatic coater and developer.

Figure 2 shows SEM (Scanning Electron

Fig. 1. First JBX-9300FS was installed at NEC Sagamihara plant in Japan. EB system is combined with in-line developer.

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Microscope) photographs of negative resist, NEB22A3 (Sumitomo Chemical Co.) for a gate fabrication and positive resist, UV5 (Shipley Co.), for contact holes exposed by 50 kV electron beam. 30-nm-width line pattern and 100-nm-diameter-hole pattern were delineated. Commercially available chemically amplified negative resist has a resolution down to 30-nm. [3]

We have investigated a mechanism for resist resolution and have developed a new type of resist, called calixarene. [4] We found that the resolution of an organic negative resist depends on the molecular size of its composed material of resist. [5, 6] The average molecular weight of an usual negative resist ranges from several thousands to several ten thousands and its molecular size or diameter ranges from a few nanometers to several tens nanometers. This resist shows a resolution of only ten nm. [7] It is important to obtain low molecular weight resin for high resolution. The roughness of the resist pattern is affected not only by molecular size of the resist but also by dispersion. [8] Calixarene resist pattern and its chemical structure is shown in **Fig. 3**. Calixarene used in this experiment consists of 6-phenol ring and has a low molecular weight of 972 with almost monodispersity. 10-nm-order resist pattern is delineated exposed at 100 kV. The resist shows ultrahigh resolution and high durability under halide plasma etching using HBr, CF_4 and Cl_2. Exposure characteristics are shown in **Fig. 4**. Sensitivity decreased as an acceleration voltage increased from 50 kV to 100 kV as a factor of 1.7. On the other hand, contrast is improved when an acceleration voltage of 100 kV compared with that at 50 kV. The sensitivities are same for the thickness of 35 and 100 nm due to high acceleration voltage.

We measured a deposited energy distribution at 50 kV and 100 kV on silicon wafer for proximity effect correction. We irradiated electron beam on NEB22A3 negative resist on silicon wafer without deflection. The deposited energy distribution in arbitrary unit is shown in **Fig. 5**. The deposited energy distribution curve for 100 kV near the beam-irradiated point is sharper and lower than that for 50 kV. This means a small forward scattering range and then a possibility of high-resolution patterning. The deposited energy distribution for 100 kV at around 10 μm is lower than that for 50 kV. This region of deposited energy depends on backscattered electrons. This deposited energy affects a long-range proximity effect. According to the results, proximity effect for 100 kV is smaller than that for 50 kV, therefore it has a possibility that high-density, high-resolution patterning is delineated by using 100-kV electron beam.

Mix-and-Match lithography

Point electron beam exposure has the advantage of high resolution, but has the disadvantage of low throughput. Therefore, EB lithography is applied for the specific layer including fine patterns such as gate layer, which cannot be delineated by optical lithography and the other layers including no fine patterns are delineated by the optical lithography. This strategy is called as Mix-and-Match lithography. [9,10,11] In this lithography, there is a problem of overlay error between patterns exposed by EB and optical lithography (stepper). JBX-9300FS has a feature called stepper distortion correction. When using this feature, distortion of field (or chip) exposed by a stepper is measured in advance and measured distortion data is stored in JBX-9300FS. Differences to an ideal position in a stepper exposure field of KrF stepper is about 30 nm for both x and y direction. When EB exposure, exposed patterns (or EB field) are distorted to be as same as that exposed by a stepper. Then high overlay accuracy is obtained between layers exposed by EB and by optical stepper. In **Fig. 6**, overlay error between patterns exposed by EB and by optical stepper with and without stepper distortion correction are shown. Due to the correction, overlay error distribution decreased from 35 to 20 and 28 to 15 nm in x and y direction, respectively. The residual average overlay error was observed due to insufficient calibration, and it can be reduced because of stable error value.

Other type of Mix-and-Match lithography is that one pattern layer is exposed by EB and optical stepper to obtain high-throughput. We call Intra-level Mix-and-Match lithography.[12] A pattern data in the same layer is divided into two, then one pattern data includes fine patterns smaller than a threshold length L_{th}

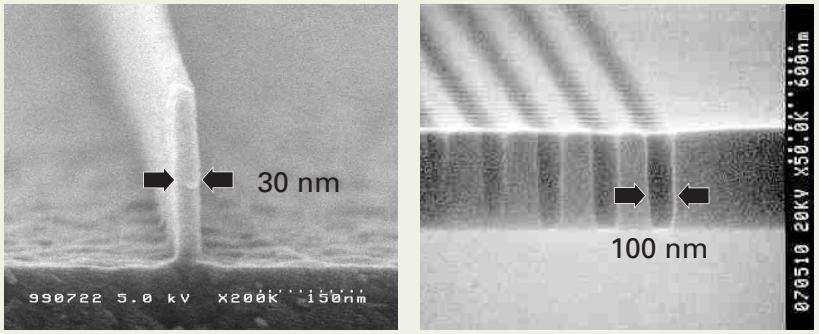

Fig. 2. Line pattern using negative resist, NEB22A3 on polysilicon layer (a) and UV5 (b) on silicon wafer exposed by 50 kV, 400 pA EB. Both are chemically amplified resist. Exposure doses are 48.4 μC/cm^2 for NEB22A3 and 28 μC/cm^2 for UV5.

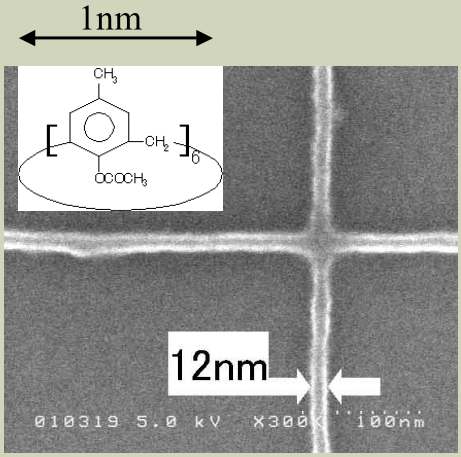

Fig. 3. High-resolution calixarene resist pattern exposed at a dose of 100 mC/cm^2 by 100 kV, 400pA beam. Resist thickness is 35 nm. Design width is 5nm.

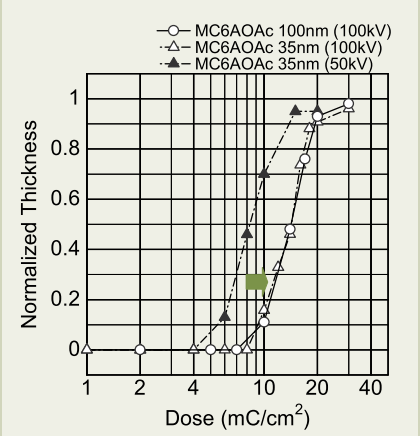

Fig. 4. Exposure characteristics of calixarene resist exposed at 50 kV and 100 kV. Resist sensitivity decreased as a factor of 1.7, but contrast increased.

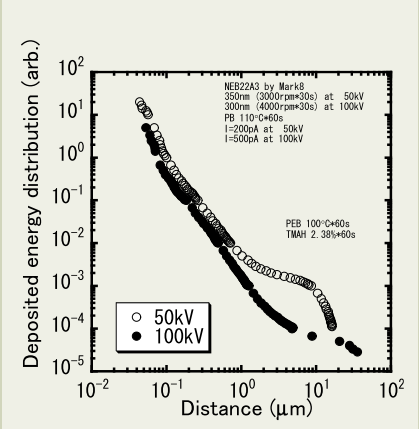

Fig. 5. Deposited energy distribution on silicon wafer at 50 and 100 kV.

as a criterion for EB exposure and the other pattern data includes rough patterns larger than L_{th} for optical stepper. In this Mix & Match lithography, it is desirable that a resist used can be exposed both by EB and optical stepper. NEB22A3 chemically amplified negative resist has high sensitivity both for EB and optical exposure, then this resist was used in our experiments.

Because there is an intrinsic pattern placement error due to each exposure tool, it is necessary to add supplementary pattern to avoid detachment between patterns exposed by EB and stepper. We developed a method to generate a supplementary pattern (overlap margin) by logical operation on figures using CAD.[11] A generation process is described in **Fig. 7(a)**. We use 'L' shape overlaps to avoid detachment both in x and y directions. First, we divide a pattern into EB and optical patterns by using threshold length L_{th}, for example, 0.16 µm. Then, we move one pattern in ΔW and extract an overlap area as an overlap. Next, we move the overlap in opposite direction in ΔW and enlarge the overlap in ΔL, and extract an overlap area again. The value of ΔW and ΔL is decided according to a relative positional error in x and y direction between EB and optical stepper. Finally, we move these overlaps in ΔW and merge the overlaps and the divided pattern. The feature of this method is that there is no pattern size limitation, and we can handle fine patterns less than ΔW. The exposed resist pattern by Mix-and-Match lithography using this overlaps generation method is shown in **Fig. 7(b)**. Large rectangle area for a gate pad and a fine line pattern for gate electrode were exposed by KrF stepper and point EB, respectively. Fine line pattern with a width of 40 nm without detachment was obtained.

The effect of Mix-and-Match lithography is shown in **Fig. 8**. Exposure area for EB decreased to 1/6 compared with an area for EB when exposed by EB exposure only. Exposure time for EB decreased to 1/3. This discrepancy in reduction ratio is due to blanking time, settling time of EB and stage motion.

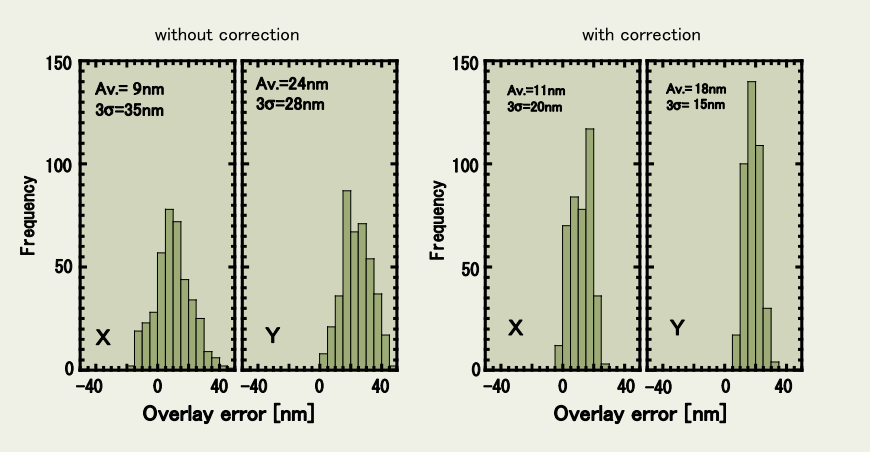

Fig. 6. The effect of stepper distortion correction is shown. Distribution of overlay error is improved by the correction.

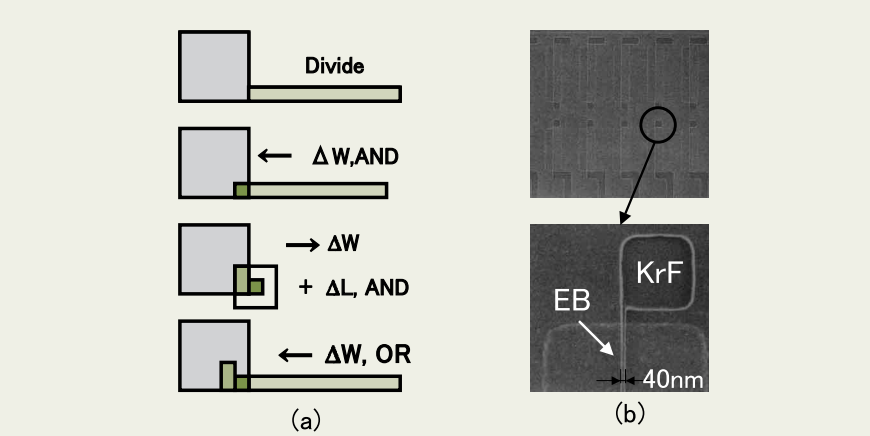

Fig. 7. (a) Process for adding overlap patterns. (b) Resist pattern exposed by Mix-and-Match lithography using EB and KrF.

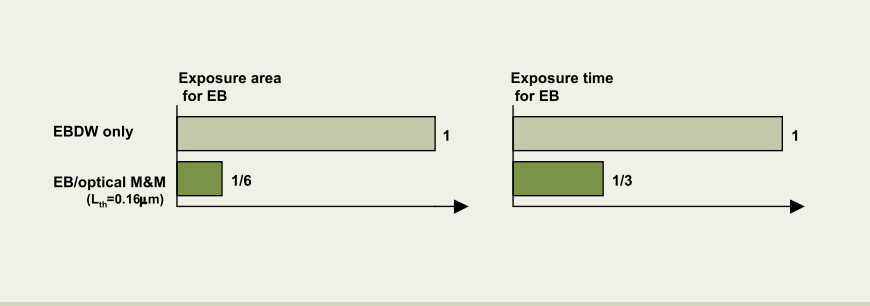

Fig. 8. The effect of Mix-and-Match lithography is shown. Exposure area for EB decreased in 1/6, and exposure time for EB decreased in 1/3.

Summary

We show lithographic performance of an advanced point electron beam system JBX-9300FS. This EB exposure system is designed for development of advanced CMOS devices with several features such as high acceleration voltage of 100 kV, large deflection field, high beam clock speed, dynamic focus/stigma correction and stepper distortion correction. Fine negative resist pattern with a width of 30 nm and positive contact hole pattern with a diameter of 100nm were obtained. We also show 10-nm-order calixarene resist pattern. We developed Mix-and-Match lithography process to increase throughput without the sacrifice of resolution. Nanolithography using JBX-9300FS is useful for development of minute devices such as CMOS and single-electron transistors.

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