

Nanometer-scale patterning of high- T_c superconductors for Josephson junction-based digital circuits

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A straightforward method for nanometer-scale patterning of high- T_c superconductor thin films is discussed. The technique combines direct-write electron beam lithography with well-controlled aqueous etches and is applied to the fabrication of Josephson junction nanobridges in high-quality, epitaxial thin-film $\text{YBa}_2\text{Cu}_3\text{O}_7$. We present the results of our studies of the dimensions, yield, uniformity, and mechanism of the junctions along with the performance of a representative digital circuit based on these junctions. Direct current junction parameter statistics measured at 77 K show critical currents of $27.5 \mu\text{A} \pm 13\%$ for a sample set of 220 junctions. The Josephson behavior of the nanobridge is believed to arise from the aggregation of oxygen vacancies in the nanometer-scale bridge.

I. INTRODUCTION

Since the development of high-quality high-temperature superconducting (HTS) thin-film materials, much effort has been expended towards the development of a manufacturable Josephson junction technology. In general, the process should have high resolution, be flexible, offer excellent dimensional control, and not damage the superconducting properties of the films. To be applicable to a digital circuit technology, the fabrication procedure must generate junctions of excellent yield and uniformity. We have developed and studied such a technology based on electron beam nanolithography and well-controlled aqueous etches. This method allows fabrication of nanobridge Josephson junctions with sub-100-nm dimensions and reasonable junction parameters. The inherent flexibility of the technique allows the fabrication of junctions at arbitrary position and orientation, resulting in minimal constraints on circuit design and with no reliance on grain boundary formation.

Several alternate technologies utilizing electron beam lithography for the direct fabrication of Josephson junctions in HTS films have been reported. One of the earliest reported techniques is that of selective epitaxy on a substrate with a patterned silicon nitride overlayer.¹ In this work, electron beam lithography is used to pattern the silicon nitride film rather than the superconductor film itself. Using this technique, $\text{YBa}_2\text{Cu}_3\text{O}_7$ (YBCO) lines down to $0.13 \mu\text{m}$ have been demonstrated but finer resolution is limited by particulate formation during deposition. Additionally, there are concerns about stress in the YBCO films and silicon outdiffusion from the silicon nitride mask.

Electron beam lithography has been used in combination with ion milling to pattern a YBCO film directly for the fabrication of microbridge Josephson junctions.² This technique is similar to that reported here, the primary differences being the use of a potentially film-damaging ion-milling etch and no demonstration of bridge dimensions below $0.15 \mu\text{m}$.

The resolution of this technique is limited in part by the need to use relatively thick resist which must withstand the ion milling. Additionally, poor junction performance was observed in microbridges with widths less than $0.3 \mu\text{m}$, attributed to damage to the superconducting properties of the film during processing.

A third technique uses a very high dose scan of an electron beam across a previously patterned YBCO microbridge to deliberately and, to some degree, controllably damage the superconducting properties in a specified region of the bridge.^{3,4} This technique has the advantage of requiring neither a resist mask nor any etching process for the actual junction formation. Among the disadvantages of this technique are the long exposure times and instability of the junction parameters over time when stored at room temperature. As reported, the exposure time per micron of microbridge width was 5–10 min compared to ~ 1 ms for a typical nanobridge reported here, a difference of more than five orders of magnitude.

The technique reported here combines direct-write electron beam lithography utilizing a thin, positive electron beam resist having an ultimate resolution smaller than 20 nm with well-controlled aqueous etchants to fabricate sub-100-nm scale nanobridges on high-quality, epitaxial YBCO. Since first reporting Josephson junction operation in YBCO nanobridges,⁵ we have continued to refine the process and to apply the technology to increasingly complex circuits. We present here the results of our studies of the dimensions, yield, uniformity, and mechanism of the junctions along with the performance of an 8-bit analog-to-digital converter containing 34 junctions.

II. NANOBIDGE FABRICATION

The as-grown YBCO films are nominally 25 nm thick and are epitaxially oriented with the c axis normal to the substrate. The typical T_c is 90 K with a critical current density

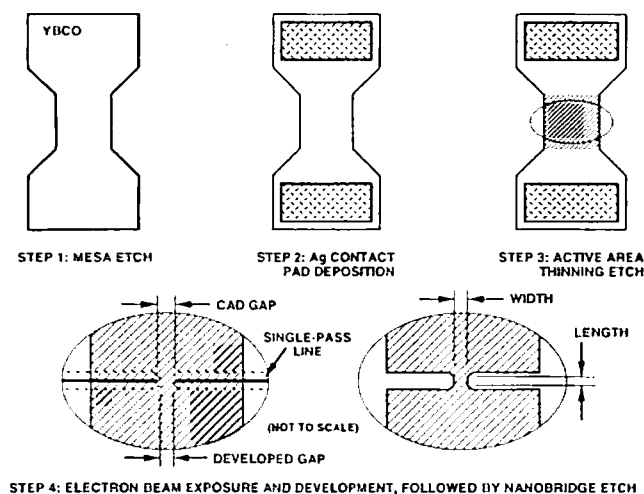


FIG. 1. The four basic process steps used in this work for the fabrication of nanobridge Josephson junctions in YBCO.

of 1 MA/cm^2 at 77 K. Details of the BaF_2 *ex situ* anneal film preparation are reported elsewhere.⁶ It is necessary that the starting film morphology be both smooth and uniform for the nanometer-scale lithography and etching to be successful.

The basic nanobridge fabrication process involves four steps depicted in Fig. 1. The four steps are (1) a mesa etch to delineate the active YBCO area, (2) deposition of Ag contacts, (3) a second etch to thin the YBCO film in the regions where the nanobridges are to be formed, and (4) exposure and etching of the nanobridges. Each of the three etching steps use ethylene diamine tetraacetic acid- (EDTA-) based wet etches. For circuit applications, a fifth step provides for deposition of normal metal as required to complete the circuits. The YBCO film in the region of the nanobridge is thinned to about 10 nm to minimize the possibility of undesirable undercutting during the etch. No systematic undercutting was observed using this technique although sometimes a random nanobridge was seen to exhibit anomalous undercutting which we attribute to an inhomogeneity in the as-grown film.

Steps (1)–(3) above are performed using standard optical contact lithography. The critical electron beam exposure step is performed using a JEOL JBX-5FE field-emission electron beam lithography system operating at 50 kV. The sample is coated with 115-nm-thick poly(methylmethacrylate) (PMMA) baked for 1 h at 170 °C. The exposure conditions include a beam current in the range of 200–800 pA, corresponding beam diameters of 5–8 nm, and beam step of 5 nm. Prior to exposure, the sample is also coated with a 10-nm gold layer to provide a current path for the incident electrons on the otherwise insulating sample. This thin gold film is removed in a standard potassium iodide/iodine (KI/I) etch prior to development. Development was performed for 60 s in 1:3::methyl isobutyl ketone:isopropyl alcohol (MIBK:IPA).

The nanobridges are defined by exposing a pair of collinear single-pass lines separated by a precisely controlled gap and centered across the thinned YBCO region (see Fig. 1).

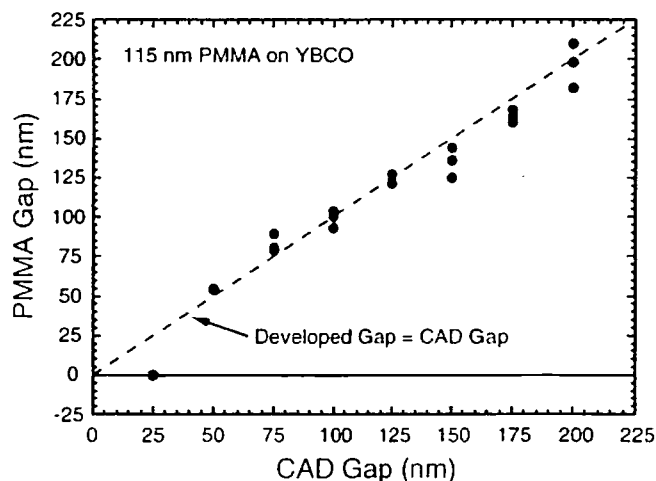


FIG. 2. Developed gap width in PMMA on YBCO as a function of CAD gap width for a fixed line dose of 2.0 nC/cm.

The gap between the lines, which determines the junction width, is defined in the computer-aided design (CAD) pattern and is limited only by the resolution of the resist and by the proximity effect. The width of the developed single-pass lines, which determines the junction length, is defined primarily by dose and by beam diameter and is limited by electron scattering effects. Developed gap width in PMMA on YBCO as a function of CAD gap width is shown in Fig. 2 for a fixed line dose of 2.0 nC/cm. This simple technique provides for excellent control of nanobridge dimensions, with developed gap dimensions falling within 10% of the CAD gap. The corresponding developed single-pass linewidth is approximately 30 nm.

Two variations of the basic nanobridge fabrication process have been used. For the earliest devices (process A), the CAD gap was varied from 0.1 to 0.2 μm and the dose was varied from 2.3 to 4.0 nC/cm. The etchant used was decarbonated disodium EDTA ($\text{Na}_2\text{H}_2\text{EDTA}$),⁷ applied in sequential steps, measuring for junction behavior after each step. A scanning electron micrograph of an etched nanobridge fabricated using process A and having sub-100-nm width and length is shown in Fig. 3. For all subsequent junctions (process B), the CAD gap is fixed at 0.075 μm and written at a fixed dose of 2.0 nC/cm. The etchant used is full strength EDTA. Because this etch causes more edge damage to the YBCO film than the $\text{Na}_2\text{H}_2\text{EDTA}$ etch, the sample undergoes a 30-min oxygen plasma treatment⁸ to repair this edge damage. It should be noted that junction behavior is observed prior to this oxygen treatment but junction parameters are significantly improved after the treatment, as discussed below.

III. EXPERIMENTAL RESULTS

Process A generated uniform, high-yield junctions whose parameters scaled closely with the physical nanobridge geometries. Critical currents (I_c) were measured to be in the range of 4 to 20 μA with critical current–normal-state resis-

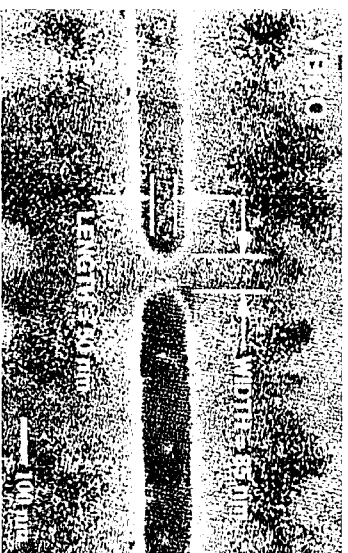


Fig. 3. Scanning electron micrograph of an etched nanobridge fabricated using process A and having sub-100-nm width and length.

lance products ($I_c R_n$) less than or equal to 100 μV at 77 K. These values are comparable to but on the low end of results for other YBCO technologies. Current-voltage curves followed the standard resistively shunted junction (RSJ) model and exhibited Shapiro steps upon application of an 11-GHz field. The magnetic field dependence of I_c is very close to the ideal $\sin(kI_c)/(kI_c)$, indicating an extremely uniform junction. Junction-to-junction uniformity of I_c was found to be $\pm 20\%$ – 25% .

Based on nanobridge dimensions alone, it is unlikely that the Josephson behavior arises from a coherence effect as in a grain boundary junction. Instead, we believe that the junction arises from an aggregation of oxygen vacancies in the nanobridge giving rise to a tunneling barrier. The very high mobility of oxygen at room temperature in YBCO has been long established.⁹ The tendency for oxygen vacancies to aggregate under an electromigration force has been reported and alternate driving forces such as stress or nearby structural defects have been suggested.¹⁰ One or both of these forces is likely present in the nanobridge, the latter from residual etch damage. The hypothesis that oxygen diffusion is the mechanism possible for junction formation is supported in our work by a simple annealing experiment. We observe that annealing of the junction in an oxygen atmosphere at 400 °C causes a significant increase in I_c (and can ultimately lead to flux-flow-like transport characteristics) as the oxygen stoichiometry in the bridge approaches that of the initial film. Figure 4 shows that the critical current then returns to roughly the preanneal value after sample storage at room temperature and atmosphere over a time scale of 24 h, suggesting the reaccumulation of oxygen vacancies in the nanobridge.

Process B also generated uniform, high-yield junctions. A representative current-voltage characteristic for a junction after oxygen plasma treatment is shown in Fig. 5. The typical critical current was less than 20 μA prior to the oxygen plasma treatment, and 25–30 μA after treatment. The post-treatment $I_c R_n$ product was typically around 250 μV at 77 K. These parameter values represent a significant improvement over the process A devices, attributed primarily to the postetch oxygen plasma treatment. The critical current value is still somewhat low for some circuit applications but this may be overcome by utilizing multiple nanobridges in parallel. We have fabricated hundreds of nanobridge junctions us-

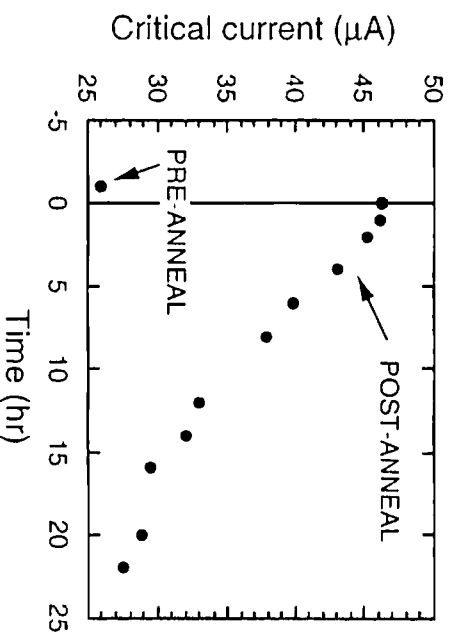


Fig. 4. Change in critical current vs time after 400 °C oxygen anneal followed by exposure to atmosphere at room temperature.

ing process B in order to study the statistics of the junction parameters. Measurements of 220 junctions from a single wafer yielded an average I_c of 27.5 μA with all I_c values falling within $\pm 13\%$ of the average. Similar data have been obtained using a more time-efficient measurement technique based on spectral analysis in the 90–170 GHz range of phase-locked, oscillating arrays of up to 2450 nanobridge junctions.¹¹ The improvement in junction-to-junction uniformity of the process B devices is attributed to improved processing, primarily better etch uniformity and the equalizing effects of the oxygen plasma healing treatment.

IV. CIRCUIT APPLICATIONS

The nanobridge Josephson junction technology has been applied to a variety of circuit applications.^{12,13} The most recent circuit to have been demonstrated is an 8-bit analog-to-digital converter (ADC) circuit utilizing 34 junctions. The circuit is composed of an input SQUID biased to the edge of the voltage state which generates a pulse stream proportional to the input current. The pulse stream is fed into a series of

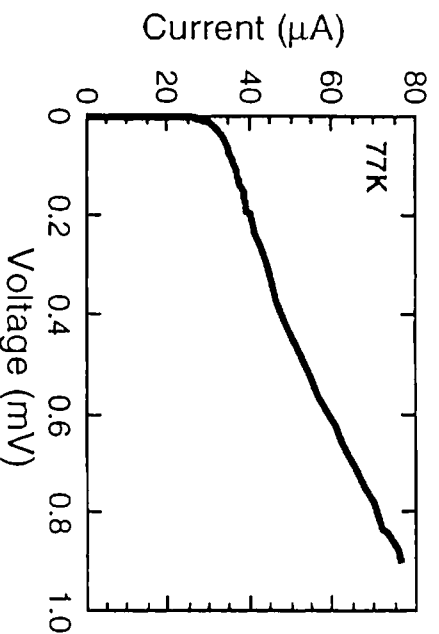


Fig. 5. Current-voltage characteristic of a process B nanobridge after oxygen plasma treatment.

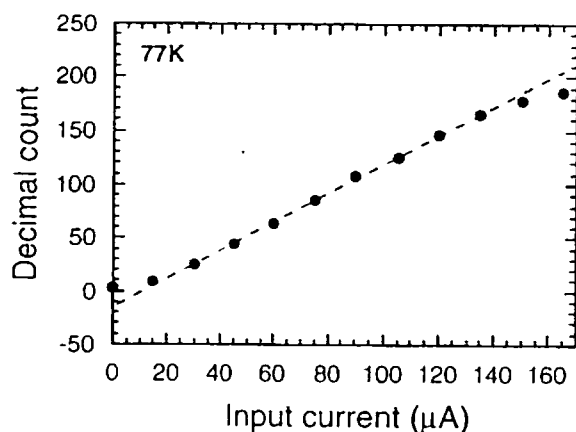


Fig. 6. Output count vs input current for the 8-bit ADC operating as a gated counter with 2-ns sample time. The linear operating range is limited by the nonlinearity in the voltage-flux curve of the input SQUID.

counter stages whose states are sensed by flux-flow amplifiers. The circuit design can tolerate up to 35% junction parameter variation which is well above that achieved with this junction technology. The output count versus input current for an 8-bit ADC operating as a gated counter with 2-ns sample time is shown in Fig. 6, revealing the linear operating range which is limited in this case by the nonlinearity in the voltage versus external flux curve of the input SQUID.

V. SUMMARY

We have demonstrated the use of electron beam nanolithography in combination with EDTA-based aqueous etches to fabricate superconducting nanobridges with sub-100-nm dimensions on high-quality YBCO films. The process provides excellent lithographic control of nanobridge dimensions and is relatively nondamaging leading to high junction yield and the highest uniformity reported for any HTS junction technology. We hypothesize that the Josephson

behavior of the nanobridges arises from the aggregation of oxygen vacancies in the nanobridge which leads to a tunneling barrier. We have demonstrated a 34-junction circuit in the form of a counting analog-to-digital converter operating with a 2-ns sample time. We believe that this fabrication technology is applicable to the further development of superconducting electronics technology.

ACKNOWLEDGMENT

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- ¹D. P. Kern, K. Y. Lee, R. B. Laibowitz, and A. Gupta, *J. Vac. Sci. Technol. B* **9**, 2875 (1991).
- ²Z. Bao, L. Ji, K. Y. Lin, B. Bi, S. Han, and J. E. Lukens, *IEEE Trans. Appl. Supercond.* **3**, 2417 (1993).
- ³A. J. Pauza, A. M. Campbell, D. E. Moore, R. E. Somekh, and A. N. Broers, *IEEE Trans. Appl. Supercond.* **3**, 2405 (1993).
- ⁴S. K. Tolpygo, S. Shokhor, B. Nadgorny, J.-Y. Lin, M. Gurvitch, A. Bourdillon, S. Y. Hou, and J. M. Phillips, *Appl. Phys. Lett.* **63**, 1696 (1993).
- ⁵J. R. Wendt, J. S. Martens, C. I. H. Ashby, T. A. Plut, V. M. Hietala, C. P. Tigges, D. S. Ginley, M. P. Siegal, J. M. Phillips, and G. K. G. Hohenwarter, *Appl. Phys. Lett.* **61**, 1597 (1992).
- ⁶M. P. Siegal, J. M. Phillips, R. B. van Dover, T. H. Tiefel, and J. H. Marshall, *J. Appl. Phys.* **68**, 6353 (1990).
- ⁷C. I. H. Ashby, J. S. Martens, T. A. Plut, D. S. Ginley, and J. M. Phillips, *Appl. Phys. Lett.* **60**, 2147 (1992).
- ⁸B. G. Bagley, L. H. Greene, J.-M. Tarascon, and G. W. Hull, *Appl. Phys. Lett.* **51**, 622 (1987).
- ⁹S. J. Rothman, J. L. Routbort, and J. E. Baker, *Phys. Rev. B* **40**, 8852 (1989).
- ¹⁰B. H. Moeckly, R. A. Buhrman, and P. E. Sulewski, *Appl. Phys. Lett.* **64**, 1427 (1994).
- ¹¹J. S. Martens, K. Char, A. Pance, L. P. Lee, M. E. Johansson, S. R. Whitely, K. E. Kihlstrom, J. R. Wendt, V. M. Hietala, T. A. Plut, G. A. Vawter, S. Y. Hou, J. M. Phillips, and W. Y. Lee, *IEEE Trans. Appl. Supercond.* **3**, 3095 (1993).
- ¹²J. S. Martens, J. R. Wendt, V. M. Hietala, D. S. Ginley, C. I. H. Ashby, T. A. Plut, G. A. Vawter, C. P. Tigges, M. P. Siegal, S. Y. Hou, J. M. Phillips, and G. K. G. Hohenwarter, *J. Appl. Phys.* **72**, 5970 (1992).
- ¹³J. S. Martens, A. Pance, K. Char, M. E. Johansson, S. R. Whitely, J. R. Wendt, V. M. Hietala, T. A. Plut, C. I. H. Ashby, S. Y. Hou, and J. M. Phillips, *IEEE J. Solid-State Circuits* **29**, 56 (1994).