45-nm Gate Length CMOS Technology and Beyond using Steep Halo

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Abstract

45-nm CMOS devices with a steep halo using a high-ramp-rate spike annealing (HRR-SA) are demonstrated with drive currents of 697 and 292 μA/μm for an off current less than 10 nA/μm at 1.2 V. For an off current less than 300 nA/μm, 33-nm pMOSFETs have a high drive current of 403 μA/μm at 1.2 V. In order to fabricate a steeper halo than these MOSFETs, a source/drain extension (SDE) activation using the HRR-SA process was performed after a deep source/drain (S/D) formation. By using this sequence defined as a reverse-order S/D formation, 24-nm nMOSFETs are achieved with a high drive current of 796 μA/μm for an off current less than 300 nA/μm at 1.2 V.

Introduction

Sub-50-nm CMOS devices have been investigated using a highly-controlled halo structure (*eg.* a super halo or a tilted channel ion-implantation) for high-performance system LSIs [1–3]. In order to precisely control the halo region, a steep halo formation, as shown in Fig. 1, is one of the key issues. Therefore it is remarkably important to suppress a thermal budget for the halo region.

In this paper, in order to suppress the thermal budget, the high-ramp-rate spike annealing (HRR-SA) process was evaluated for the halo, deep source/drain (S/D) and S/D extension (SDE) regions. Furthermore, the reverse-order S/D (R-S/D) formation with the HRR-SA process was investigated to reduce the thermal budget of a gate-sidewall formation for the halo and SDE regions. Feasible sub-50-nm CMOS devices with the steep halo structure were also performed.

Experiment

After a shallow trench isolation (STI) formation, well and channel regions were formed. A SiON gate dielectric film with $Tox_{inv}^{n/p}$=2.5 nm was used by an NO oxynitridation. A gate pattern of a 270-nm thick EB-resist was exposed by a mix-and-match (M&M) lithography with over-lap regions, using a point electron-beam (EB) (JBX-9300FS) and a KrF, as shown in Fig. 2 [4]. After an *in-situ* EB-resist thinning, a gate-etching process was carried out, as shown in Fig. 3. A fine gate electrode down to 24 nm was implemented by these techniques.

The halo, SDE and S/D regions were performed by the R-S/D and C-S/D formations under the HRR-SA condition. The HRR-SA process has a fast ramp-up rate of 300 °C/sec and an approximately fast ramp-down rate of 100 °C/sec. In contrast, a spike annealing (SA) process has a slower ramp-up rate of 75 °C/sec and a slower ramp-down rate of 35 °C/sec. A $CoSi_2$ film of 7 Ω/sq. was formed after a final gate-sidewall-formation. In order to suppress a diffusion and de-activation of halo and SDE dopants, the back-end process was carried out at a lower-temperature less than 700 °C.

Results and Discussion

A. Conventional-Order S/D (C-S/D) Formation

In order to suppress the thermal budget for the halo and SDE regions, the HRR-SA process was performed [5, 6]. The HRR-SA process at 1050°C improves a short channel effect (SCE) for n/pMOSFETs, as shown in Fig. 4. However, drive currents (I_{ON}) at an off current (I_{OFF}) of 10 nA/μm decrease with a decrease in the HRR-SA temperature from 1050 to 1030 °C, as shown in Fig. 5. This is caused by both a parasitic resistance increase and a gate-electrode depletion.

In order to effectively suppress the SCE, a halo-ion-implantation (I/I) dose was optimized using a 1050-°C HRR-SA process, as shown in Fig. 6. 45-nm CMOS devices with a lower off-current less than 10 nA/μm are performed by a high-dose halo for n/pMOSFETs, as shown in Figs. 7 and 8. Figure 9 shows the I_{OFF}-I_{ON} characteristics for n/pMOSFETs with various halo doses at 1.2 and 1.5 V. The drive currents at an off current of 10 nA/μm are almost the same for all halo

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doses in the C-S/D formation. Excellent cut-off and I_D-V_D characteristics are achieved for n/pMOSFETs with a gate length of 24-45 nm, as shown in Figs. 16 and 17. The drive currents for 45-nm n/pMOSFETs are 697 and 292 $\mu A/\mu m$, respectively, for the off current less than 10 $nA/\mu m$ at 1.2 V. Moreover, the high drive current of 403 $\mu A/\mu m$ is achieved for 33-nm pMOSFETs with the off-current less than 300 $nA/\mu m$ at 1.2 V. However, a severe reverse-SCE (RSCE) is observed for the high-dose-halo n/pMOSFETs, as shown in Fig. 6.

B. *Reverse-Order S/D (R-S/D) Formation*

In order to sufficiently improve both the SCE and the drive current, the R-S/D formation was implemented using the HRR-SA process. The RSCE, SCE and threshold voltage (Vth) fluctuation are dramatically suppressed by the R-S/D formation for nMOSFETs, as shown in Fig. 10. Furthermore, a drain induced barrier lowering (DIBL) and a subthreshold swing (SS) values are drastically suppressed by the R-S/D formation for less than 50-nm nMOSFETs, as shown in Fig. 11. These results indicate that a transient enhanced diffusion (TED) and a thermal diffusion (TD) are effectively suppressed by a low temperature gate-sidewall formation after the halo and SDE formations in the R-S/D formation. On the other hand, the pMOSFETs using the R-S/D and the C-S/D formations have almost the same Vth lowering, as shown in Fig. 10. Figure 12 shows the off current dependence on a physical gate length for nMOSFETs. I_{OFF}-degradation slope for a fine gate length less than 50 nm is remarkably suppressed using the R-S/D formation. I_{OFF}-I_{ON} characteristics are drastically improved using the R-S/D formation, as shown in Fig. 13. It is speculated from these results that the halo and SDE profiles using the R-S/D formation are steeper than those using the C-S/D one.

The relationship between an HRR-SA annealing temperature and device characteristics was evaluated for n/pMOSFETs using the R-S/D formation, as shown in Fig. 14. A minimum gate length (Lmin) at the off current of 10 $nA/\mu m$ decreases with a decrease in an HRR-SA temperature, however, the drive current is seriously suppressed, because of only a parasitic-resistance increase. In contrast, the drive currents using the R-S/D formation significantly increase with an increase in the halo dose, compared to those using the C-S/D formation, as shown in Fig. 15. It has been reported that high drive currents are maintained by the steep SDE profile using a low temperature annealing process [7]. Therefore this result in this paper indicates that the steep SDE and halo profiles are obtained by the R-S/D formation with the HRR-SA process. Excellent cut-off and I_D-V_D characteristics are achieved for 24-nm nMOSFETs, as shown in Figs. 16 and 17. The high drive current of 796 $\mu A/\mu m$ is observed for 24-nm nMOSFETs with the off-current less than 300 $nA/\mu m$ at 1.2 V.

C. *Device Performances*

Figure 18 shows the propagation delay time (τ_{pd}) dependence on a harmonic mean of the drive current for an inverter ring oscillator using the CMOS devices with F/O=1 at 1.2 and 1.5 V. The τ_{pd} values are almost the same for the R-S/D and the C-S/D formations. On the other hand, the R-S/D formation remarkably suppresses the τ_{pd} values for the same gate length, compared to the C-S/D formation, as shown in Fig. 19. The τ_{pd} values for the R-S/D formation are 26% faster than those for the C-S/D one. This is because the drive current formed by the R-S/D formation for nMOSFETs is higher than those by the C-S/D one. Therefore 11.7 psec/stage is achieved at 1.2 V.

Conclusion

Sub-50-nm CMOS devices down to 24 nm with a lower off current are demonstrated by the steep halo using the R-S/D or C-S/D formations with the HRR-SA process at 1.2 V. The drive currents for 45-nm n/pMOSFETs using the C-R/D formation are 697 and 292 $\mu A/\mu m$ for an off-current less than 10 $nA/\mu m$, respectively. For the off-current less than 300 $nA/\mu m$, the drive currents for 33-nm pMOSFETs using the C-S/D formation are 403 $\mu A/\mu m$. Furthermore, 24-nm nMOSFETs using the R-S/D formation have high drive currents of 796 $\mu A/\mu m$ for the off-current less than 300 $nA/\mu m$. Finally 11.7 psec is achieved for F/O=1.

Acknowledgments

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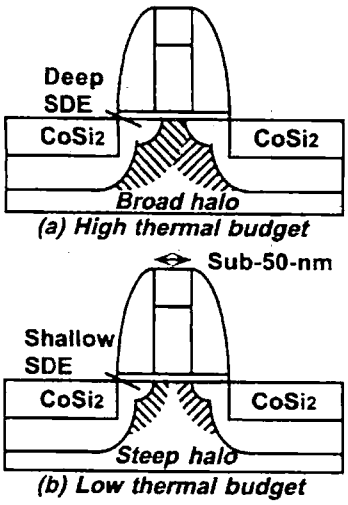

Fig. 1: Schematic design concept for steep halo using low-thermal-budget process.

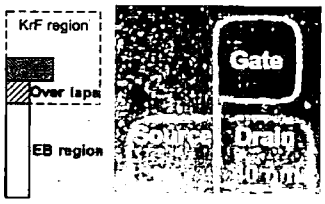

Fig. 2: Plane SEM photo of gate pattern using point-EB/KrF Mix&Match lithography.

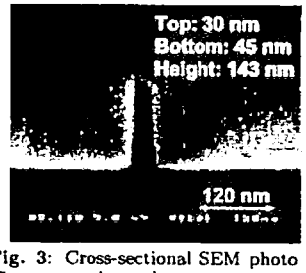

Fig. 3: Cross-sectional SEM photo for 45-nm gate electrode.

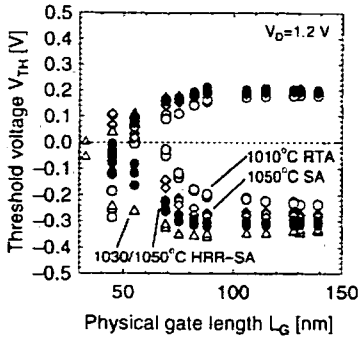

Fig. 4: Threshold voltage dependence on physical gate length for n/pMOSFETs as a function of S/D annealing process.

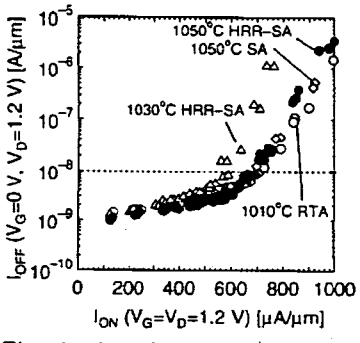

Fig. 5: I_{OFF}-I_{ON} characteristics for nMOSFETs with various S/D annealing processes.

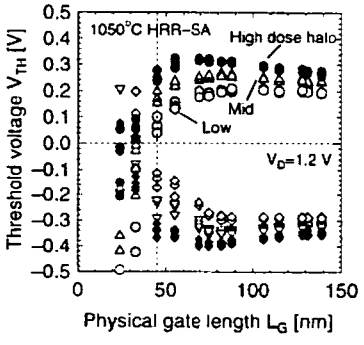

Fig. 6: Threshold voltage dependence on physical gate length for n/pMOSFETs as a function of halo dose.

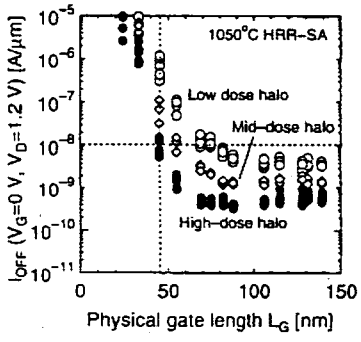

Fig. 7: I_{OFF} dependence on physical gate length for nMOSFETs with various halo doses.

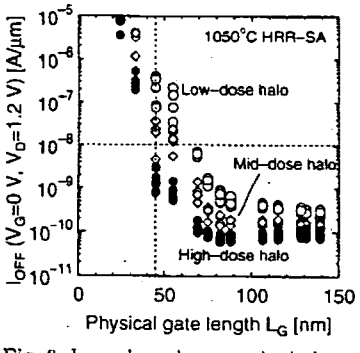

Fig. 8: I_{OFF} dependence on physical gate length for pMOSFETs with various halo doses.

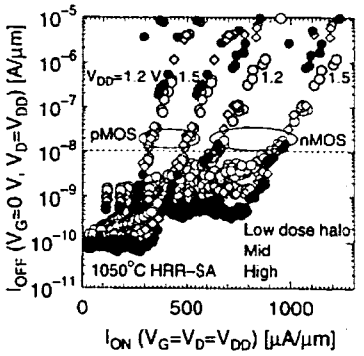

Fig. 9: I_{OFF}-I_{ON} characteristics for various-halo-dose n/pMOSFETs.

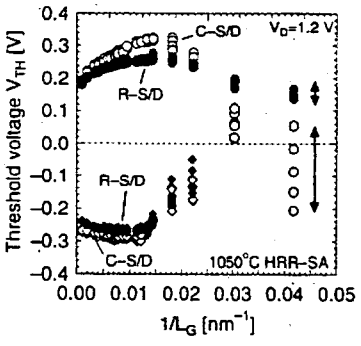

Fig. 10: Threshold voltage dependence on inverse of L_G for n/pMOSFETs using reverse-order S/D (R-S/D) and conventional-order S/D (C-S/D) formations.

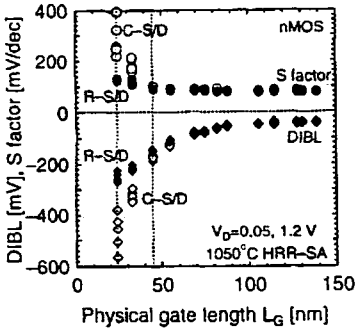

Fig. 11: DIBL and S-factor characteristics as a function of gate length for nMOSFETs using R-S/D and C-S/D formations.

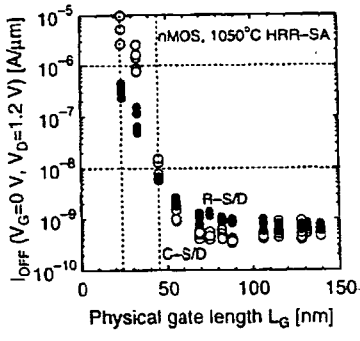

Fig. 12: I_{OFF} dependence on physical gate length for nMOSFETs using R-S/D and C-S/D formations.

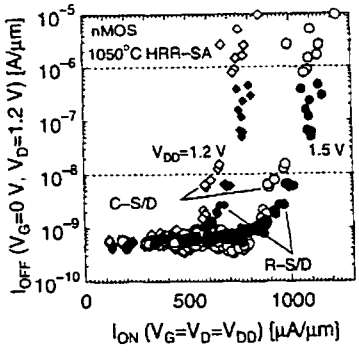

Fig. 13: I_{OFF}-I_{ON} characteristics for nMOSFETs using R-S/D and C-S/D formations.

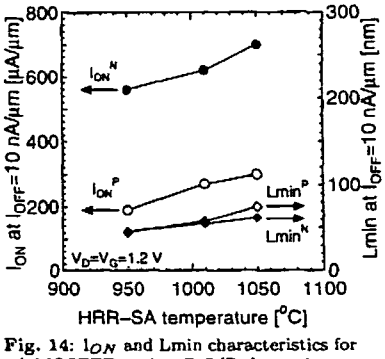

Fig. 14: I_{ON} and Lmin characteristics for n/pMOSFETs using R-S/D formation as a function of HRR-SA temperature.

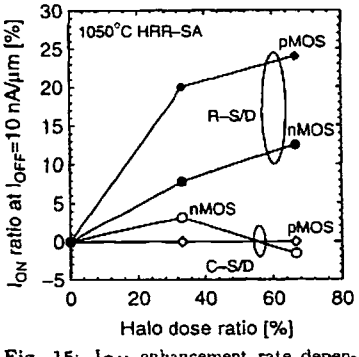

Fig. 15: I_{ON} enhancement rate dependence on halo-dose ratio for n/pMOSFETs using R-S/D and C-S/D formations.

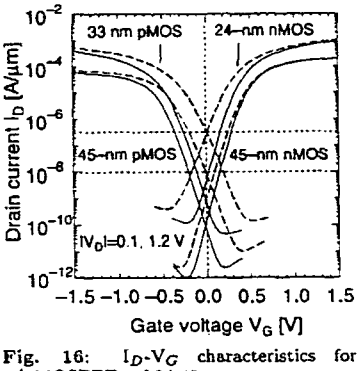

Fig. 16: I_D-V_G characteristics for n/pMOSFETs of 24-45 nm.

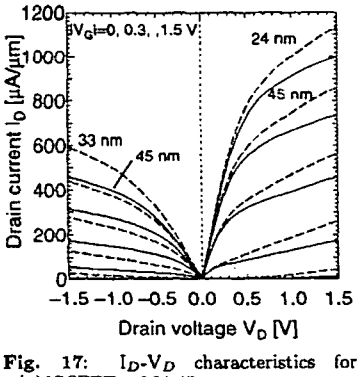

Fig. 17: I_D-V_D characteristics for n/pMOSFETs of 24-45 nm.

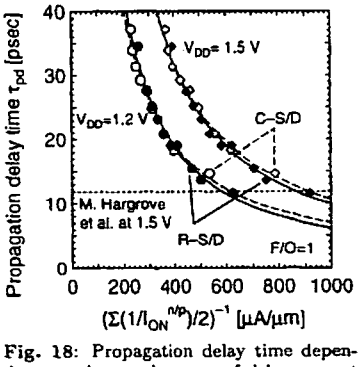

Fig. 18: Propagation delay time dependence on harmonic mean of drive current for inverter ring oscillator using CMOS devices with F/O=1 at 1.2 and 1.5 V.

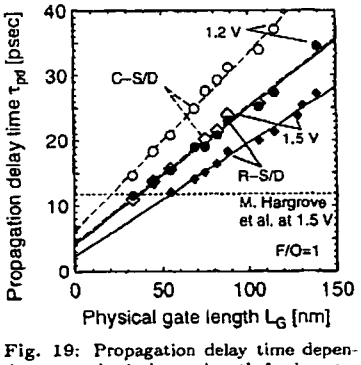

Fig. 19: Propagation delay time dependence on physical gate length for inverter ring oscillator using CMOS devices with F/O=1 at 1.2 and 1.5 V.